NEW POWER CONVERTER TOPOLOGIES FOR MINIMIZING ENERGY CONSUMPTION OF ELECTRONIC APPLIANCES

A Thesis
Presented to
The Academic Faculty

by

Ravishankar Nilakantan

In Partial Fulfillment
of the Requirements for the Degree
Master of Science in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
August 2011

NEW POWER CONVERTER TOPOLOGIES FOR MINIMIZING ENERGY CONSUMPTION OF ELECTRONIC APPLIANCES

Approved by:

Dr. Deepak Divan, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. A.P. Sakis Meliopoulos
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Santiago Grijalva
School of Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: August 2011

ACKNOWLEDGEMENTS

I would like to thank my advisor Dr. Deepak Divan for giving me the wonderful opportunity to work with him on this project and for his exceptional guidance. I would also like to thank the committee, Dr. Sakis Meliopoulos and Dr. Santiago Grijalva for their time.

During the course of my masters I had the opportunity to exchange ideas with many of my fellow students who helped me a great deal in my research. I would especially like to thank Debrup Das, Rajendra Prasad Kandula, Rohit Moghe and Ramkumar Hariharan. I would like to thank Dr. Frank Lambert for providing me the opportunity to conduct crucial tests at NEETRAC. I would also like to thank James Steinberg for providing me with the means for creating the final product for this thesis. I would especially like to thank the Electric Power Research Institute (EPRI) for sponsoring this work and providing constant support to me throughout the term of this thesis.

I would like to thank my parents and grandparents for their continued love and support which has been a constant source of motivation and encouragement to me during the course of my study.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

PC	Personal Computer
SMPS	Switch Mode Power Supply
ESR	Equivalent Series Resistance
dc	Direct Current
ac	Alternating Current
ZVS	Zero Voltage Switching
ZCS	Zero Current Switching
SRC	Series Resonant Converter
PRC	Parallel Resonant Converter
SPRC	Series Parallel Resonant Converter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	Negative channel Metal Oxide Semiconductor
SR	Synchronous Rectifier
SPSR	Smart Power Synchronous Rectifier
RMS	Root Mean Square
HD	High Definition
LCD	Liquid Crystal Display
MFP	Multi Functional Printer
SSSR	Self Sustained Synchronous Rectifier

LIST OF SYMBOLS

LLC	Resonant tank configuration with two inductors and a capacitor
LCC	Resonant tank configuration with two capacitors and an inductor
V_f	Forward Voltage drop across a diode
I_{LOAD}	Load Current
P_{cond}	Conduction Loss
$V_{f\text{-}sync}$	Forward Voltage drop across a synchronous rectifier
$R_{DS\ (ON)}$	On State Resistance of the Synchronous MOSFET
I_{SW}	Current through the Switch (MOSFET)
I_L	Load Current
V_{AK} ,V_{KA}	Voltage across the terminals A and K of a diode
I_g	Gate Current
R_g	Gate Resistance
Q_g	Gate Charge
η	Efficiency
f_{SW}	Frequency of Switching
T	Time Period of Switching
ON	Device is conducting
V_{CC}	Positive Voltage Supply Rail
V_{ee}	Negative Voltage Supply Rail
V_{REF}	Reference Voltage
I_{REF}	Reference Current
V_O	Output Voltage
V_O	Output Voltage

Vin	Input Voltage
t_f	Fall time of current during turn OFF of MOSFET
I_c	Current through the Input Power Switch
$I_{c\ (start)}$	Current I_c during the start of a switching cycle
$I_{c\ (final)}$	Current I_c during the end of a switching cycle
$I_{d\ (avg)}$	Average current through the output diode rectifier
P_{total}	Total Power
I_{iload}	Internal load of the SSSR
I_{ch}	Charging current
V_{C2}	Voltage across the storage capacitor C2
P_{CD}	Power consumed by the internal load of the SSSR fed by V_{CC}
ΔE	Energy delivered in one switching cycle
V	Volts
A	Ampere
Wh	Watt Hour
kWh	Kilowatt Hour
GWh	Giga Watt Hour
TWh	Tera Watt Hour
mW	milli Watt
MW	Megawatt
CO_2	Carbon dioxide
secs	seconds
mins	minutes
kHz	Kilo Hertz

SUMMARY

The proliferation of electronic equipment that is permanently connected to the grid causes significant parasitic losses. Yet, the design of power supplies for PCs, servers, multi-function printers, etc, is governed by the cost and component specifications at the peak operating point as well as the thermal management of the power supply itself. For example, most power supplies have lower efficiencies at light loads than at their rated loads. If the unit spends most of its time at the light load operating point, then the energy consumption will be much higher compared to a situation where the power supply is optimized for overall energy consumption with a specified load cycle. Considering that most electronic appliances are produced in high volume, the use of power supplies that permit easy custom design makes sense from the standpoint of energy efficiency. Over the past few years, multiple topological changes and design changes that aim to improve the efficiency of the power supplies have been proposed. However, their proliferation in low cost consumer electronics has been limited primarily by their high costs, additional area overhead and incompatibility with existing power supply converter topologies. As a part of this Master's thesis research work, a business case is first proposed to show that a market for low cost and high power rating electronic devices that exhibits high power efficiency exists. Then a novel yet simple, low cost solution is proposed to improve the efficiency of existing power supplies without effecting major changes to their existing design. Our claims are backed up by simulation results and a working prototype. Finally, a ROI model is presented to showcase the effectiveness of the proposed solution in today's consumer market.

CHAPTER 1

INTRODUCTION

1.1 Motivation

In recent years the number of appliances loading the power supply of a household has increased tremendously. These appliances work on dc power whereas the power grid supplies ac power. Hence, either an internal or an external power supply is made use of to convert the power grid ac voltage to the required dc voltage levels. Most of these loads are plugged in to the wall permanently and hence cause significant parasitic losses even when inactive; such losses are referred to as standby losses. The power supplies used in electronic appliances aren't designed for maximum power efficiency; instead, their design is driven by cost considerations, optimum performance at the appliance's peak operating point, and the thermal efficiency of the power supply. Such a design methodology results in low light load efficiencies which presents an issue since modern appliances spend most of their time in standby, which translates to a light load condition. Therefore, owing to the design of power supplies for peak operating point efficiency, the energy losses of electronic appliances is a lot higher than it should be. Thus, a strong case exists for a better and more adaptable design of power supplies used by electronic appliances.

1.2 Problem Statement

The main aim of this project is to develop cost effective and power efficient power supply design solutions that exhibit improved matching of load requirements over the defined operating cycles. The main benefit would be to eliminate the additional energy losses that occur during an electronic appliance’s standby mode of operation or light load condition. It is also imperative that the solutions developed be minimally intrusive and easily adaptable to the existing power supplies without incurring a high

design overhead.

CHAPTER 2

LITERATURE REVIEW

The first part of this chapter provides the basis for the need of a standard and also an overview of the standards used in measuring and quantifying the energy efficiency of power supplies.

The second part of the chapter provides a brief introduction to the power converter topology designs that are widely used today. This is followed by an analysis of a few designs that were proposed to improve the efficiency of these topologies. This analysis will explain the inability of these ideas in solving the issue mentioned in the problem statement.

The third chapter includes an explanation of the concept of a synchronous rectifier followed by an analysis of existing solutions that deploy the synchronous rectifier. Also, designs that predate our proposed solution are re – visited with the view of validating the usefulness of the new solution.

2.1 Measurement and Quantification of the Efficiency of Power Supplies

The continued introduction of multiple power converter topologies that drive widely varying loads at different voltage levels necessitates the creation of a standard procedure for the measurement of power supply efficiency. This procedure would fulfill the dual purpose of helping the consumer in making an informed decision when purchasing a power supply and in helping the power supply designer in understanding the power supply requirements better. In addition to these two basic purposes the standardization also helps in quantifying the energy being lost in the power supplies on a nationwide scale and in understanding the benefits and effects of mitigating this loss. There exist numerous independent third party test and rating agencies which oversee the

measurement and quantification of the efficiency of the power supplies and rate their energy efficiency with programs such as ENERGY STAR.

The procedures to test the power supplies consistently and accurately across different testing benches have been laid out in [1] and [2].

2.1.1 Measurement Test Setup

The generic test setup to measure the efficiency of the power supply is proposed in [3] and is shown in Figure 1.

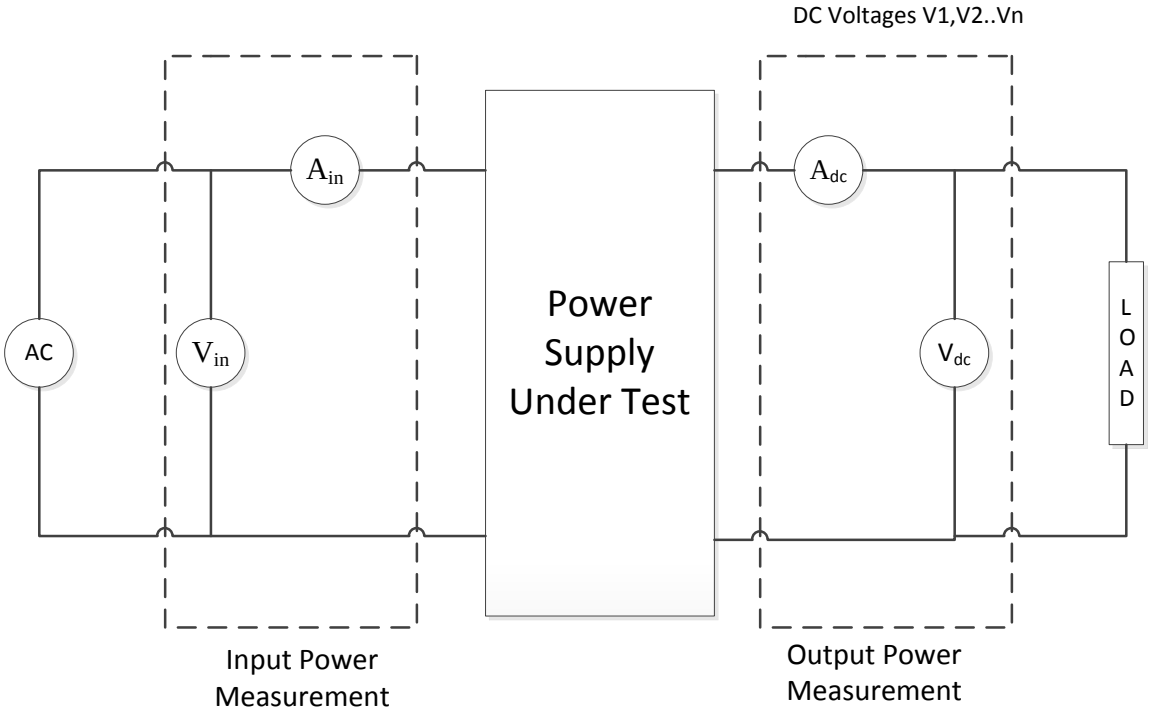


Figure 1: Generic Test Setup to Measure the Efficiency of Power Supplies [3]

The test setup consists of an ac voltage source on the input side which supplies the input power to the power supply under test. The variation in the input voltage should not be more than ±0.1% of the specified source voltage value and the THD should not exceed 2% up to and including the 13th harmonic [2]. The power supply is to be suitably loaded according to the testing procedures by an appropriate rheostat or another suitable dc current source. The dc loads must draw current with an accuracy of ± 0.5% within the

current loading set point for each output voltage. The power measurements are to be made with suitably calibrated voltmeter and ammeter or power meters; measurements of power 0.5W or greater should be made with an uncertainty of less than 0.5% at a 95% confidence level. The input power is to be computed using an averaging technique over a minimum of 32 input cycles and dc measurements for voltage should have an uncertainty of less than 0.1% and corresponding current measurements should have an uncertainty of less than 0.5%.

2.1.2 Loading Procedure

The loading criteria for single output voltage systems is simple and based on rated dc output current and not on rated dc output power i.e. 25% loading of a 100W,5V,20A system means the current source is adjusted to draw 5A of current from the system. However for multiple output voltage systems the loading procedure is not as simple and requires use of sophisticated methods. A loading criteria based on a proportional allocation method proposed in [3] to load power supplies with multiple output voltages is explained in this section. According to the proportional allocation method each output is loaded proportionally i.e. 20% loading means each of the outputs are loaded to 20% of their full load output value (e.g. a 5V, 20A output is loaded to 4A and a 12V,10A output is loaded to 2A. Derating is applied in cases where the sum of individually maximum outputs exceeds the total rated output of the power supply.)

The proportional allocation method in loading the power supplies helps in standardizing the efficiency measurement procedure, but it has the disadvantage of being too general i.e. in applications where the power supply is always disproportionally loaded (e.g. one output is loaded more than the other outputs.) this test procedure fails to provide an accurate model of the actual conditions under which the power supply is operating and hence the measured efficiency does not correlate with the actual operating efficiency of

the power supply. A different method to measure the efficiency of multiple output power supplies for specialized applications is provided in section 3.2.

2.2 Identification of Existing and Proposed Power Converter Designs

The general block diagram of an ac-dc switch mode power supply operating in open loop is shown below in Figure 2.

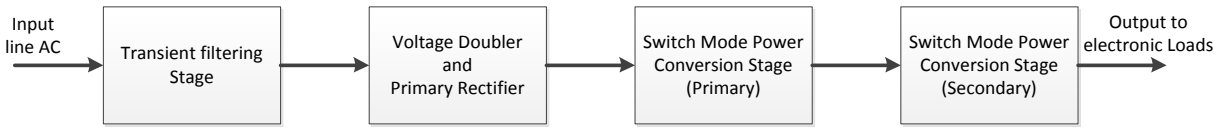


Figure 2: Basic Block Diagram of a Commercial Switch Mode Power Supply

The switch mode power supplies used in the electronic appliances consists of four main operational stages. They are:-

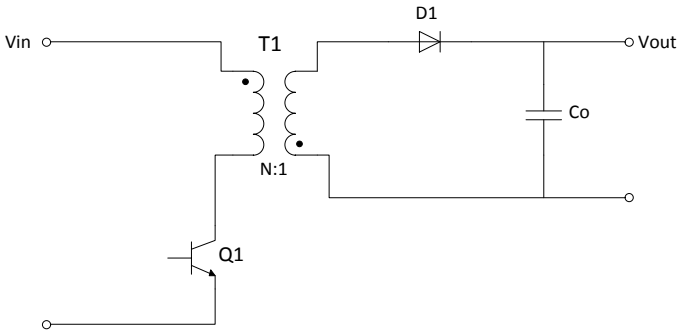
1. **Transient Filtering Stage** - The input line ac is filtered to remove the grid transients and to prevent the noise generated from within the circuit from entering into the power line.
2. **Voltage Doubler and Primary Rectifier** - This stage doubles the voltage if the ac input source used is 110V and proceeds to rectify and filter this ac voltage.
3. **Switch Mode Power Conversion Stage (Primary)** – One of the many dc-dc power converter topologies is used in a switching configuration in this stage. They convert the rectified output (dc) from the previous stage into high frequency ac.
4. **Switch Mode Power Conversion Stage (Secondary)** – The outputs from the previous stage are stepped down using a high frequency transformer and then rectified, filtered and outputted to the electronic loads.

The transient filtering and the voltage doubler stages consists of filter elements like ferrite coils, inductor, capacitors, resistors and protection elements like fuses. So the power loss in these circuits are minimal and limited to just the losses in their equivalent series resistance (esr). The primary rectification stage consists of diodes and capacitors which rectify and filter the input ac into dc. The diodes in this stage conduct current only for a very small period of time, once in every 10-15 cycles depending on the value of the input capacitor. Hence the losses in this stage are also small. From this it appears that the majority of the power lost in the switch mode power supply is in the switching elements of the power converter stage.

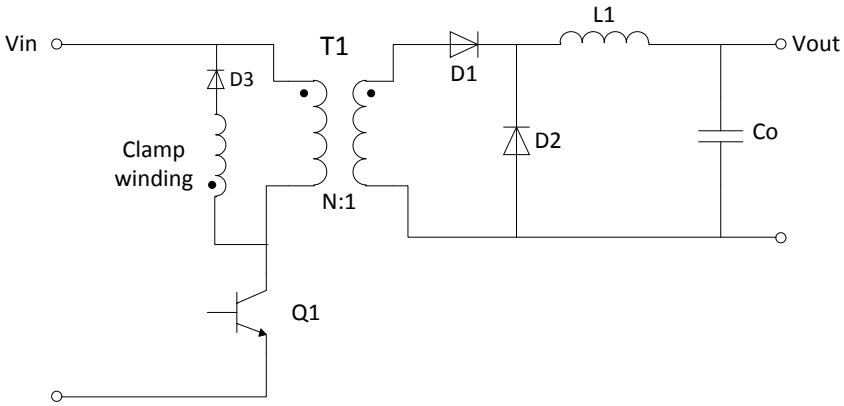
The configuration of the circuit and the topology of the SMPS [4] in these two stages (three and four) forms a crucial part of the power supply as it determines how the power will be transferred to the output. The transformer, inductors, capacitors and power semiconductors are arranged in different configurations to form different topologies.

2.2.1 Basic Power Converter Topologies

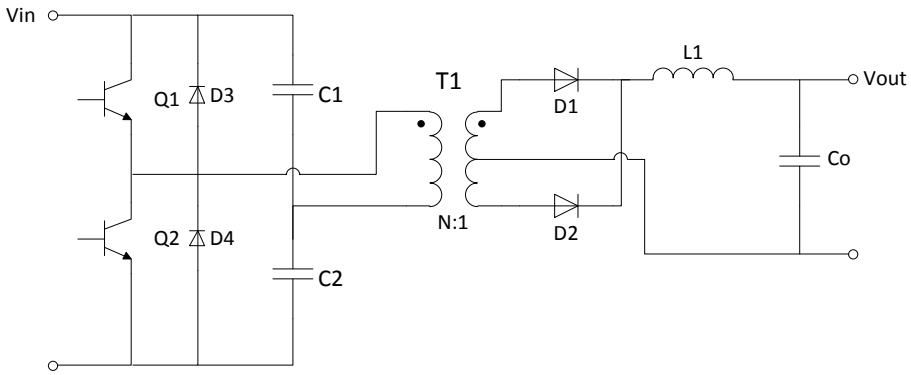
The most basic and simple power converter topologies are the buck, boost and buck-boost. Almost all the other topologies in use today are derived from these basic topologies. However these basic converters cannot be used in commercial power supplies since they lack a basic component i.e. the high frequency power transformer which is crucial in providing isolation between the power line and the highly sensitive electronic loads along with voltage scaling capabilities and the ability to supply multiple outputs. The five most common SMPS converter topologies in use today are the fly back, forward, push-pull, half-bridge and full-bridge types. They are variations of the basic buck, boost and buck-boost converters used with a high frequency transformer. The circuit diagrams of the simple single output fly back, forward and half-bridge converter topologies are shown below in Figure 3 [5].



(a)



(b)



(c)

Figure 3: Common Power Converter Topologies (a) Fly back Converter (b) Forward Converter (c) Half-Bridge Converter.

Although each of these circuits shown above has their own advantages and disadvantages, they share some common features. All the three configurations have power switches in the primary, a high frequency transformer, diodes in the secondary for rectification and filter inductor and capacitors in the output. The efficiency of these power converter topologies range from 75-80% [4]. The major elements which contribute to the power loss are the input primary power switches and the output rectifier diodes. The losses are split between the power switch conduction loss, switching loss in the power switch and the output diode conduction loss.

Switching loss is directly proportional to switching frequency. However, the size and cost of the filter components and transformer decrease with the switching frequency. As mentioned before, the emphasis in on the meeting of cost, space and thermal constraints rather than on efficiency in the design of the power supply. So if not for the thermal limiting factor that comes with increased switching losses, the switching frequency in commercial power supplies would have been increased to the physical limits of power switches.

2.2.2 Improved Power Converter Topologies

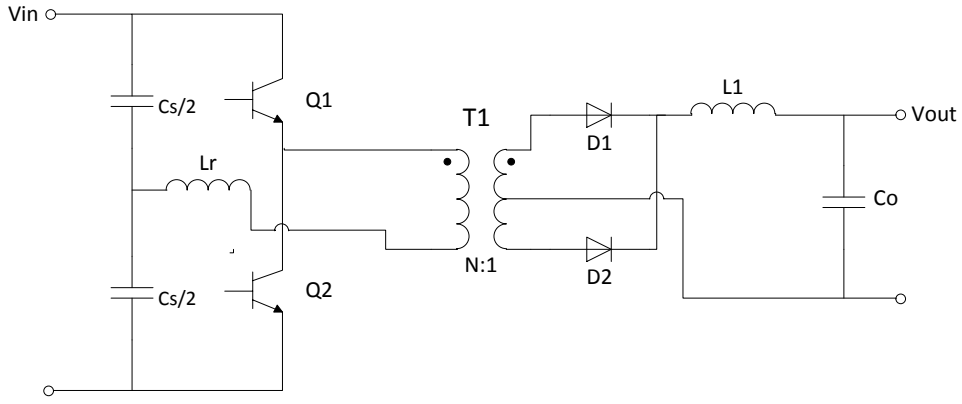
A lot of research has been done to improve the efficiency of power supplies. The proposed methods choose to improve the efficiency either by using additional components on the existing power converter topologies or by developing new topologies.

2.2.2.1 Resonant Topologies

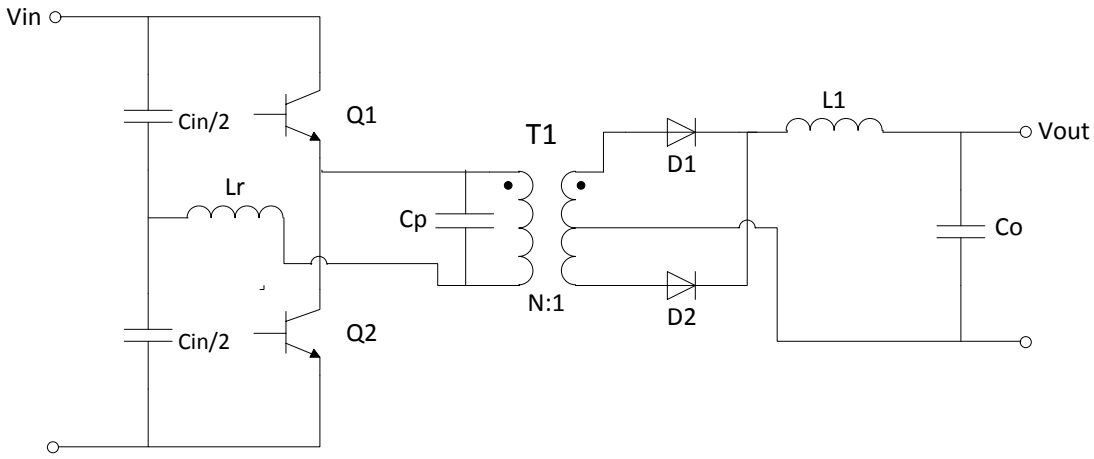
An effective method to meet the twin specifications of high switching frequency and reduced losses would be to develop topologies that reduce the switching losses. This can be achieved with the use of resonant topology converters as they can be operated at high switching frequencies with high efficiency. The resonant converters achieve lower switching losses by controlling the switching instant of the power-semiconductors such that they turn on and off with either zero voltage across them or while conducting zero

current through them. The former is referred to as zero voltage switching (ZVS) and the latter is called zero current switching (ZCS) [5].

The three basic types of resonant converters applied to half bridge topology are the series loaded resonant converter (SRC), parallel loaded resonant converters (PRC) and the series–parallel loaded resonant converters (SPRC). They are shown below in Figure 4.

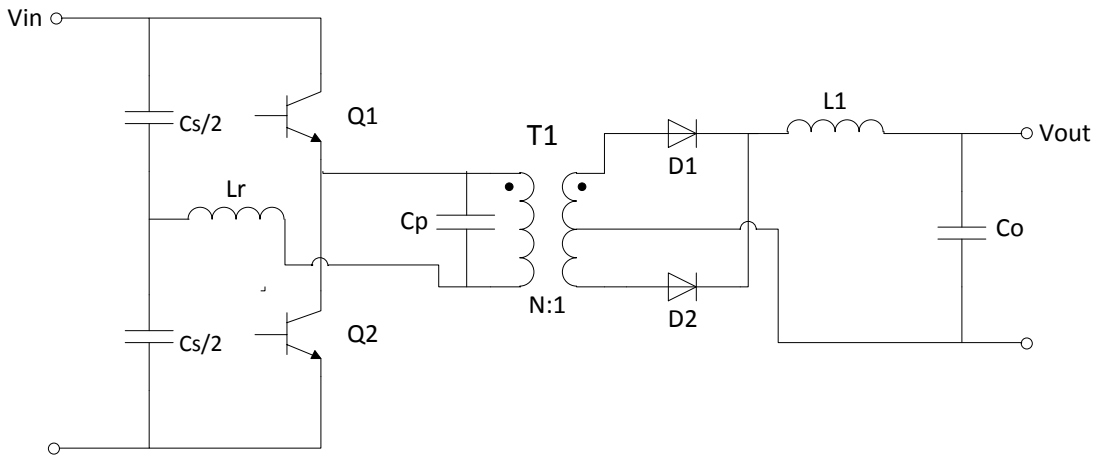


(a)



(b)

Figure 4: Basic Types of Half-Bridge Resonant Converter Topologies (a) Series Resonant Converter (b) Parallel Resonant Converter (c) Series-Parallel Resonant Converter.



(c)

Figure 4 continued: Basic Types of Half-Bridge Resonant Converter Topologies (a) Series Resonant Converter (b) Parallel Resonant Converter (c) Series-Parallel Resonant Converter.

The series loaded resonant converter topology uses the two capacitors Cs/2 to form a series-resonant capacitor Cs which along with the inductance Lr forms the series resonant circuit [6]. In the parallel loaded resonant converter [7], Cp, the resonant capacitor, and the two capacitors in the input side, Cin/2, are used to split the input dc voltage. The series-parallel loaded converter [8] has both the series and parallel-resonant capacitors.

All these three resonant converters help in mitigating the switching losses. When comparing the series and parallel resonant converters, the main advantage of the series resonant circuit is that the current in the circuit decreases as the load decreases which is not the case in the parallel loaded circuit where the converter current is independent of the load current. Hence, the series topology has better part load efficiency [9]. However, the parallel converter has better no-load regulation compared to the series loaded converter. The series-parallel loaded converter (SPRC) combines the advantages of both the series and parallel loaded converters. However the SPRC cannot provide the same

efficiency characteristics over a wide input voltage and load range [10]. The LLC converter [11] mitigates that problem by providing effective zero voltage switching over a wide input and load range. There have been numerous variations of resonant converters that have been proposed over the years to better match the characteristics of the desired application with the appropriate converter.

Although the use of resonant topologies helps in reducing the switching losses tremendously, they increase the current and voltage stresses on the power devices as the power switches are forced to carry twice the rated voltage or current depending on the topology of the resonant converter. This necessitates the use of higher rated and more expensive switches and also increases the conduction losses in the power devices. The use of any type of resonant topology requires redesign of the existing converter, use of additional parasitic components and more complex design and control strategies. All these factors deter the use of these topologies in the already space constrained, low cost power supplies.

2.2.2.2 Improving Power Supply Efficiency by modifying existing design.

A lot of research has been done on improving the efficiency of the power supply by modifying the existing circuit configurations with the use of additional components, clever design, better control strategies etc. However, most of these design changes are extremely topology specific i.e. they propose to improve the efficiency of only a particular topology and require significant changes in the circuit to do so. E.g. The efficiency of the forward converter can be improved by using a common-source active clamp circuit to suppress the switching surges and to realize soft switching [12] or by shifting to a double forward converter or fly back/forward converter topologies which are more efficient designs compared to the simple forward converter [13]. Similarly the efficiency of a fly back converter can be improved by using a non-complementary active clamp method that proposes to recycle the energy in the leakage inductance of the

transformer and achieve soft switching in the power switch [14] or by using a modified higher efficiency fly back converter design [15].

Although these designs propose to improve the efficiency of the power supplies, they are highly topology dependent and cannot be implemented on a large scale. They also require significant additional components like an extra clamp circuit, additional switches etc and are only low impact solutions since they don't improve the efficiency by a significant amount.

2.2.2.3 Improving the light load efficiency of Power Supplies

The switching losses in the power supply increase with increasing switching frequency. The effect of switching loss is more pronounced at light loads leading to efficiency degradation at low loads. This effect is more severe at higher switching frequencies. A simple way to improve the light load efficiency is to decrease the switching frequency during light loads. However reducing the switching frequency may cause the operating frequency to enter into the human audible range and hence will result in production of noise [16] and as the electronic appliances spend most of their time in the standby mode (light load operation) this method will cause extreme discomfort to the consumer. Another method to decrease the losses is to use an auxiliary power supply which is optimized for light load operation [16]. So during the normal mode of operation the main power supply operates and during the light load mode it is completely turned off relinquishing its operation to the auxiliary power supply. However, this is a very expensive solution.

The most common method that is being proposed today is the Burst Mode of operation [16]-[18]. In power supplies that use this method, the control strategy devised is such that during the active mode of operation, the PWM controller operates as usual. However, when the load decreases below a certain limit, the controller enters into the burst mode of operation. In this mode of operation, the switch is gated for a few cycles to

build the current in the output. After the current has been built, the gate is turned off for a significant portion of time until the current falls below a certain limit after which the power switch is gated again. This kind of operation effectively reduces the switching frequency and hence the losses. The effective switching frequency is reduced to be around several hundred Hz as the human ear is most sensitive to frequencies around 2kHz. This reduces the audible noise produced by the circuit while effectively reducing the switching losses as well.

This mode of operation is effective in improving the power supply's light load efficiency by reducing the switching losses during part load. However it mandates the use of a current sensing circuit and complex control strategies and designs to ensure that the switching between the two modes of operation is smooth and free of oscillations. This increases the cost of design of the power supplies and hence the effective cost of the power supply. These factors act as deterrents to the rapid adoption of this technology into the low cost power supply market.

All the methods we have discussed up to this amount are either high impact but expensive solutions or low impact solutions and hence cannot be adopted by the highly competitive low cost power supply market. All these methods propose to improve the efficiency of the power supply by reducing the switching losses in the primary side power switches. However, a major chunk of the losses in the power supply occur in the diode rectifier on the output side of the power converter. The conduction loss in the diode rectifier makes up almost all of the secondary side losses. The conduction loss in the diode rectifier is given by the formula $P_{cond} = V_f \times I_{load}$ where V_f is the forward voltage drop of the diode and I_{load} is the output load current. As the load current increases, the conduction losses also increase. The losses can be reduced by using diodes with very low forward voltage drop e.g. Schottky diode. The Schottky diode has a low forward voltage drop of 0.5 - 0.6V and so it has been prominently used in the power supplies as the diode rectifier. However the efficiency is limited by the inherent lower bound on the forward

voltage drop of the diode. The forward voltage drop is in series with the output voltage and hence in low voltage high current applications this drop almost entirely dominates the efficiency of the power supply because as the output voltage drops, the rectifier forward drop becomes comparable to the output voltage itself [19]. To further decrease this forward voltage drop, synchronous rectification can be used.

2.3 Synchronous Rectification

The synchronous rectifier is an electronic switch that provides a low on-state resistance path. It helps in improving the power conversion efficiency when placed across or instead of the diode by providing a low on state resistance conduction path [20], [21]. Generally MOSFETs are used as the electronic switch; specifically the n-channel MOSFETs (NMOS) are preferred owing to their low on state resistance $R_{DS\ (ON)}$ and are operated in their third quadrant of operation. The forward voltage drop across the synchronous rectifier unlike the diode rectifier is dependent on the load current (as $V_{f\text{-}sync} = I_{load} \times R_{DS\ (ON)}$). So as the load current increases, the voltage drop across the synchronous switch also increases. At light loads, the synchronous rectifiers are more effective as the forward voltage drop across them is very low compared to their diode counterparts. The Figure 5 shows the comparison between the forward voltage drop across the diode and the synchronous rectifier for different load currents.

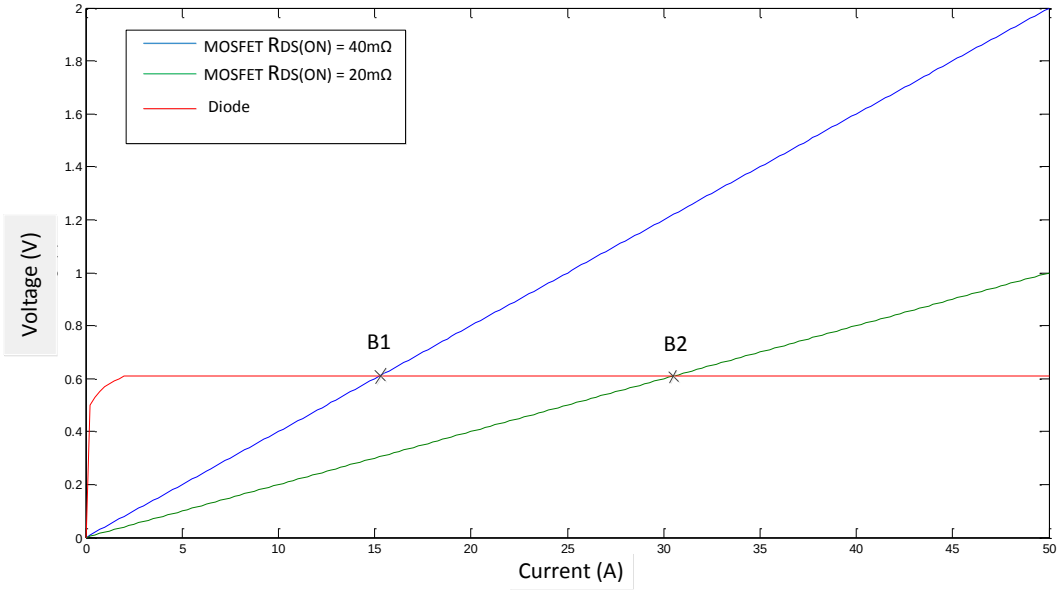


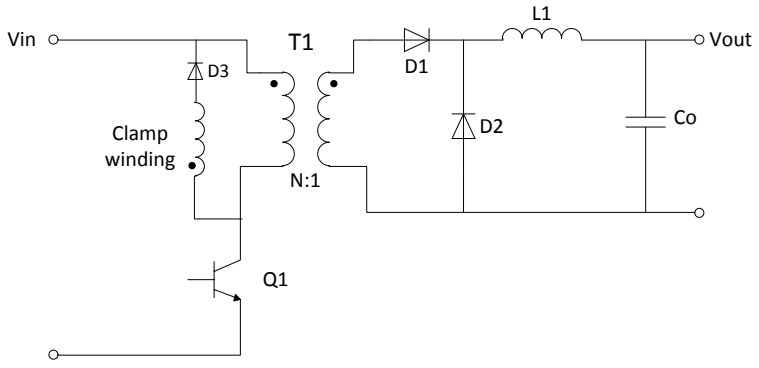
Figure 5: Comparison of the Forward Voltage Drop across the Synchronous Switch and the Schottky Diode.

The break even current is the current that has to be carried by the MOSFET to ensure that the forward voltage drop across it exceeds the forward drop of the diode. From the Figure 5 we can see that for a diode with forward drop of 0.6V and a synchronous switch with $R_{DS\ (ON)}$ of 40mΩ, the break even current B1 is 15A. As the $R_{DS\ (ON)}$ of the switch drops, the amount of current it can carry while providing better characteristics than the diode increases. So under light load conditions the conduction losses from the synchronous switch is significantly lower than the conduction loss of the diode. Also the switching loss in the synchronous rectifier is negligible since in most cases the synchronous rectifier is controlled to turn on and off when the body diode across it is conducting and hence this results in ZVS switching. Allowing the body diode of the MOSFET to conduct in this fashion may cause significant conduction loss as its characteristics is not good. So a low current schottky diode may be paralleled with the rectifier to provide the advantages of both ZVS switching and low conduction loss.

As the output voltage drops, the effect of using a synchronous rectifier (SR) on the efficiency of the power supply becomes more prominent since the SR facilitates a lower voltage drop in series with the output than compared to the diode. For e.g. using an SR with 20mΩ $R_{DS\ (ON)}$ rather than a 0.6V V_f diode in a 5V, 10A power supply results in an efficiency improvement of 8% at full load whereas the same SR provides an efficiency improvement of 12% while supplying the 10A load at 3.3V. Other than output voltage and load current the synchronous rectifier's efficiency gain also depends on its switching frequency and the input voltage (as this determines the duty cycle and hence the time of conduction of the synchronous rectifier). Higher input voltage and lower switching frequency improves the advantage of the SR. The gate drive also influences the efficiency gain of the SR. Driving an SR with a lower voltage gate drive can help in reducing the gate loss (gate loss is proportional to the gate drive voltage), however the effects of increase in $R_{DS\ (ON)}$ with decreased gate drive voltage (and hence less enhanced MOSFET) must also be taken into consideration.

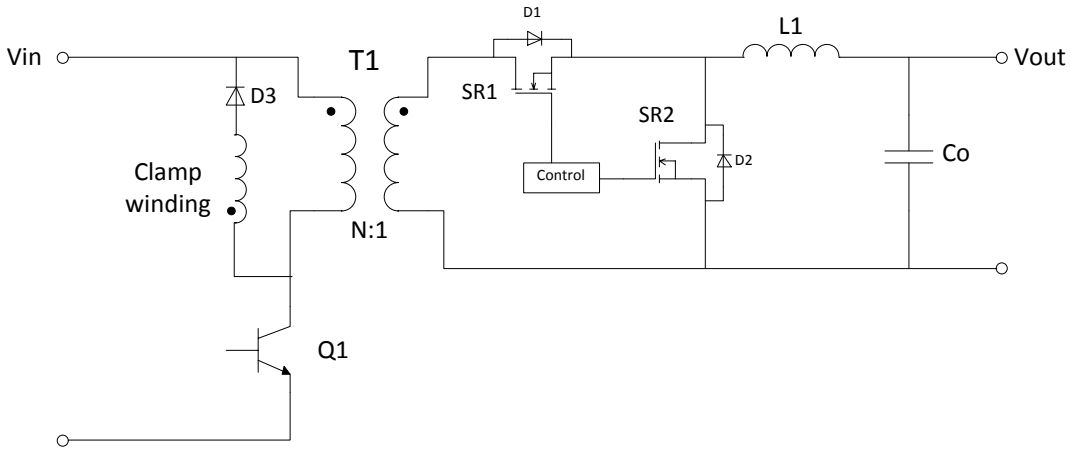
2.3.1 Implementation of the synchronous rectifier

The Figure 6 below shows a basic forward converter implemented with a diode rectifier and with a synchronous rectifier.



(a)

Figure 6: Forward Converter Implemented using (a) Diode as Output Rectifier (b) Synchronous MOSFET as the Output Rectifier.



(b)

Figure 6 continued: Forward Converter Implemented using (a) Diode as Output Rectifier (b) Synchronous MOSFET as the Output Rectifier

The synchronous switches SR1 and SR2 in the Figure 6(b) need to be controlled in such a way that the switches operate as if they were diodes i.e. when the voltage across SR1 becomes positive, the control to SR1 needs to turn it on and when the voltage across it becomes negative, the control needs to switch SR1 off.

The simplest implementation of the synchronous rectification is the self-driven synchronous forward converter. In this implementation the gates of the synchronous rectifiers SR1 and SR2 are cross-coupled to the secondary voltage of the transformer T1 and directly driven by the secondary voltage [22]. The self-driven synchronous forward converter is shown below in Figure 7.

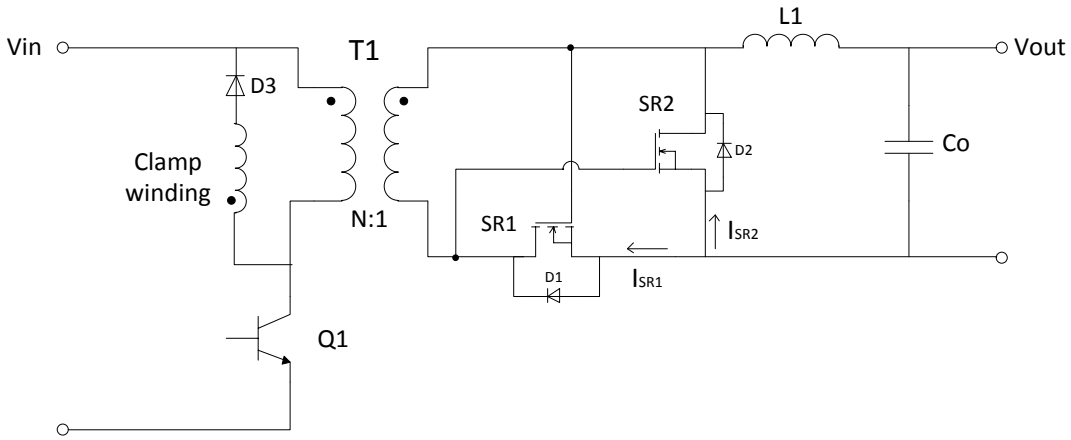


Figure 7: Self-Driven Synchronous Forward Converter [22].

This is referred to as the simplest implementation of the synchronous rectifier since it does not require external drive or control circuitry to provide the gate signals. But the performance of the SR strongly depends on the voltage waveform appearing across the transformer secondary. So even though the self-driven synchronous rectifier looks simple to implement, it has some serious drawbacks. This method of controlling the SR is highly topology dependent i.e. it can be used only with the forward converter topology and so it is not possible to extend this method easily to control other topologies. Also the gate drive voltage depends directly on the transformer voltage and this causes extensive losses in the gate drive (if the transformer voltage is high) and acts as a limiting factor in cases where the transformer voltage exceeds the maximum gate drive voltage of the synchronous rectifier. The circuit would then require additional control circuitry to limit the gate voltage thus complicating the already complex power supply circuit. And additionally the self-driven method of controlling the synchronous rectifier requires changing the power supply board to accommodate the new connections and hence further complicates the power supply board design. All the above stated reasons prevent the wide scale adoption of the self-driven synchronous rectifier.

The more widely used method of controlling the synchronous rectifier is the control driven SRs. In this method the synchronous rectifier switches are controlled using gate drive signals derived either from the primary switch gate drive or from an independent secondary control circuit. When the gate drive signals are obtained from the primary, the controller has the overall system information and hence knows when each SR has to be turned on and off. No additional voltage or current sensing circuits are required in this case since the primary controller has the data as to the state of each switch in the circuit. The main drawback of using a central primary controller is that in the power supply, the primary circuit is completely isolated from the secondary circuit by the high frequency transformer and hence additional isolation circuits (isolation transformer, optocoupler or digital isolation circuits) are required to deliver the signals from the primary controller to the secondary synchronous rectifier. This may introduce significant delay in the control signals in addition to the cost of the new isolation circuits, control design change and power supply board re-design.

The other method to implement the control driven SRs is to use completely independent control circuits directly on the secondary. This eliminates the need for isolation and thus any delay in the control signals. However it poses a new problem as in this case the independent control circuit does not have any knowledge as to when to switch the synchronous rectifier. Generally the synchronous rectifier complements the operation of the primary switch. In the case of the primary integrated control, the primary controller provides complementary signals to the primary switch and the corresponding synchronous rectifier with a dead time in between (to prevent simultaneous conduction of both the primary switch and the synchronous rectifier). However, the independent synchronous controller does not know when the primary semiconductor is switching and hence requires additional sensing circuits to determine the instants at which the synchronous rectifier should be turned on or off.

There are several ways for the independent controller to detect the instants at which they have to turn on and off the SRs. One method is to detect the voltage across the SR [23]. The block diagram of a control chip using the voltage sense method to control the SR is shown below in Figure 8.

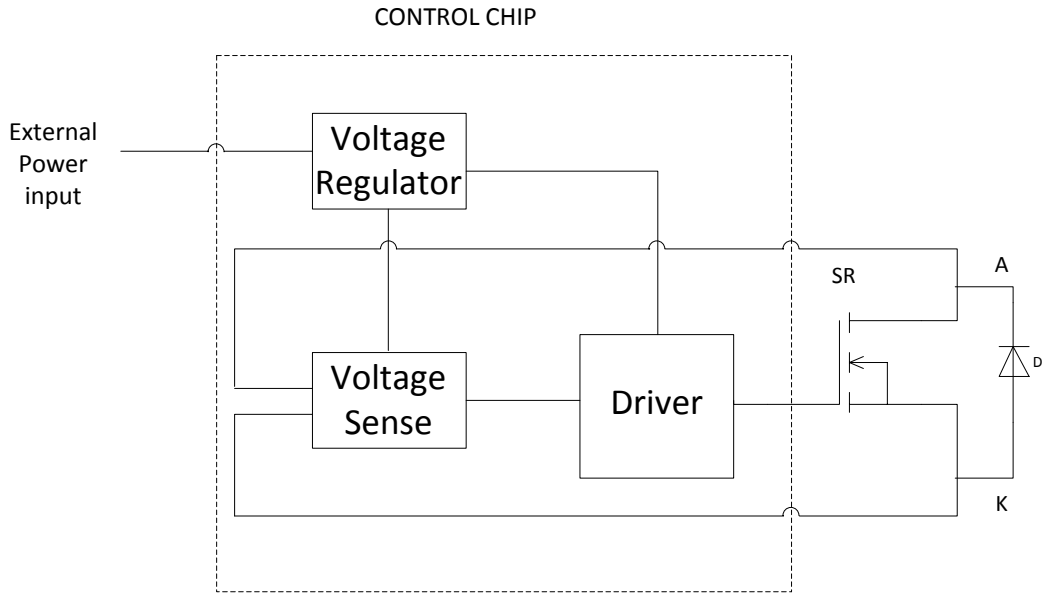


Figure 8: A Self-Driven Synchronous Controller Chip [23].

The voltage sense block of the control chip detects the instant at which the voltage across the device SR V_{AK} becomes negative and turns on the SR at that instant. There is a small delay time between the sensing instant and when the switch actually turns on during which the body diode D conducts and this results in diode conduction loss. A common strategy to mitigate this effect is to parallel a schottky diode across the switch SR. Similarly the controller turns off the switch SR when the voltage across the device V_{AK} becomes positive. The voltage sense technique is preferred over current sensing [23] as the current sensing may cause false triggering of the SR (The turn off transient may cause the SR current to oscillate around zero and hence may cause a false turn on of the SR).

Another method of design of the controller for the SR is proposed in [24]. Here, the controller detects the voltage across the secondary winding of the transformer in the first cycle of operation, stores the information to determine the switching instants and uses this information to generate the appropriate control signals for the SRs during the power supply's next cycle of operation. This method allows the controller to accurately switch the SR and helps in minimizing the dead time and hence the losses in the power supply. During the very first cycle of operation, the controller lets the body diode of the SR to conduct. The main drawback of using these methods is that they require separate control IC's. The IC's and their relevant circuit and interconnections take up precious space in the power supply board and require a re-design of the power supply circuit board.

With advances in semi-conductor technology, next generation of integrated circuits are being developed which propose to integrate both the power MOSFET and their relevant control circuitry into the same IC [25]-[26]. Though these developments are moving in the right direction (to minimize the circuit overheard required in implementing the SR) , most of these IC's still require output feedback or synchronization with the inputs along with external power which again brings back the problem of space constraints in the power supply circuit board.

2.3.2 Smart Power Synchronous Rectifier

In [27], [28] a smart power synchronous rectifier (SPSR) has been proposed which is essentially a two terminal device that is capable of replacing the diode in the rectifier directly and completely. The device contains its own sense circuitry, gating control and drive circuits and hence does not require any extra connections to the external circuit. A basic block diagram of the SPSR is shown below in Figure 9.

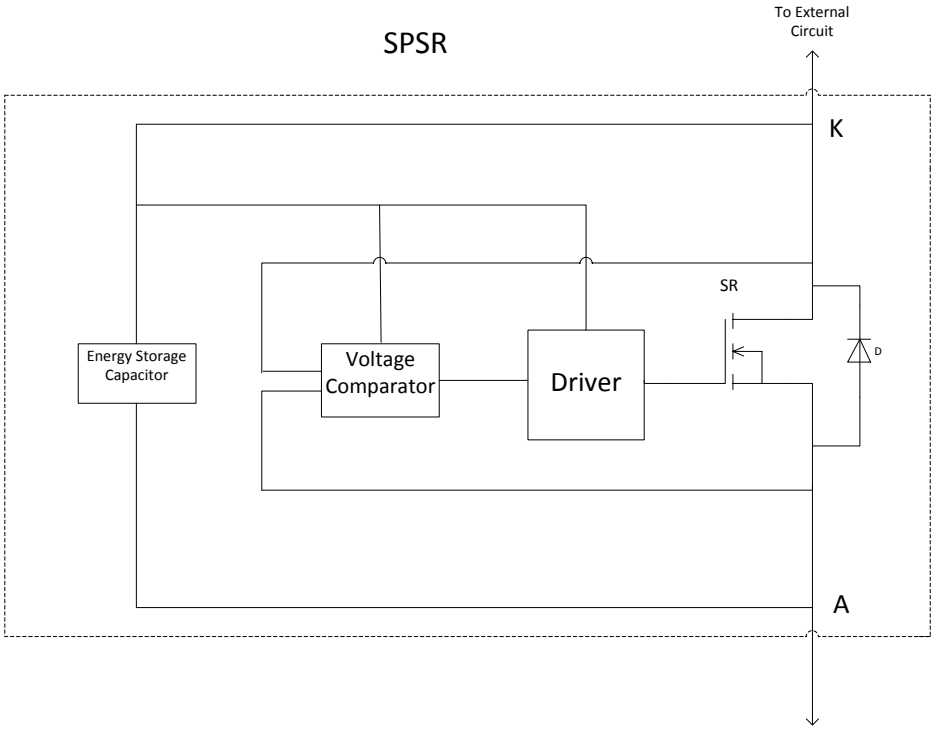


Figure 9: Block Diagram of the Smart Power Synchronous Rectifier (SPSR)

The operation of the SPSR is very simple and straightforward. The SPSR tries to emulate the operation of the diode which it is replacing. When the voltage V_{AK} across the device starts becoming positive, the voltage comparator senses this and turns ON the synchronous switch SR. Since the SR has a lower on-state voltage drop, it clamps the body diode to the voltage across itself and prevents the body diode from turning ON. When the voltage V_{AK} becomes negative, the switch SR is turned OFF. The power to the voltage comparator and the driver circuits is supplied by the energy storage capacitor. The capacitor charges when the voltage V_{AK} is negative (or V_{KA} is positive) and it discharges when the voltage V_{AK} becomes positive. Since the frequency of operation of the external circuit is generally high (> 100's kHz), a small capacitor is sufficient.

The main advantage of using a completely integrated synchronous rectifier is that the SR becomes a feasible and viable alternative to the diode as it provides higher efficiency and does not take valuable space in the power supply circuit board anymore. It

doesn't require the redesign of the existing circuit. The SPSR also provides better performance in terms of faster transient response and precise gate switching.

However the SPSR is designed specifically for low voltage applications such as on-board power supplies. The voltage across the device can not vary much as it is directly used to supply the logic circuits as well as the drive circuits. Problems that arise specifically in higher voltage applications such as input over voltage are not addressed here. Another major issue with the SPSR is that the synchronous switch in it operates over the full load current range and hence the SR has to be rated for the full load current. So a bigger MOSFET at a higher cost is required to be used as the SR. Also, since the SR has to operate over the full load range, the $R_{DS\ (ON)}$ of the synchronous switch has to be very low so that the voltage drop across the SR is lower than the forward drop of the diode even under full load condition. However lowering the on state resistance $R_{DS\ (ON)}$ means increasing the output capacitance of the device and also the gate charge. Increasing the output capacitance and the gate charge results in increased switching losses which play a major role at light load currents [29]. Hence the light load performance of the SPSR is significantly lower than its peak load performance and so the SPSR is not the suitable device to use to improve the light load efficiency of the power supplies.

Taking into account all the previous work that have been studied in the literature a new device will have to be built that improves the light load efficiency of the power supplies keeping in mind the cost and space constraints.

2.4. Summary

This chapter starts by providing a basis for the need of a new standard and an overview of the standards used in measuring and quantifying the energy efficiency of power supplies. The second part of the chapter introduces the different power converter topology designs that are widely in use today. This is followed by an analysis of the

design changes that have been proposed to improve the efficiency of the power supply and their deficiencies. The final section includes an explanation of the concept of a synchronous rectifier followed by an analysis of existing solutions that deploy the synchronous rectifier. Also, designs that predate our proposed solution are re – visited with the view of validating the usefulness of the new solution.

CHAPTER 3

MEASUREMENT OF EFFICIENCY AND ESTIMATION OF ENERGY WASTED IN COMPUTER POWER SUPPLIES

This chapter deals with the measurement of efficiency of computer power supplies that exist in the market today, computing their energy waste projections on a nationwide scale and determining whether it's feasible to improve the existing power supply design such that the energy losses in them can be minimized.

3.1 Efficiency Measurement of Computer Power Supply.

The efficiency of the power supplies used in desktop computers has been measured in the past and such testing methods have been documented in the literature study presented in section 2.1. However, the existing techniques are extremely generic and do not provide an accurate representation of the operating efficiencies of the computer power supplies and will be shown to be so in section 3.2. In this chapter, a different method for measuring the efficiency of computer power supplies is defined. The block diagram of the setup used to record the efficiency of the computer power supplies is shown below in Figure 10.

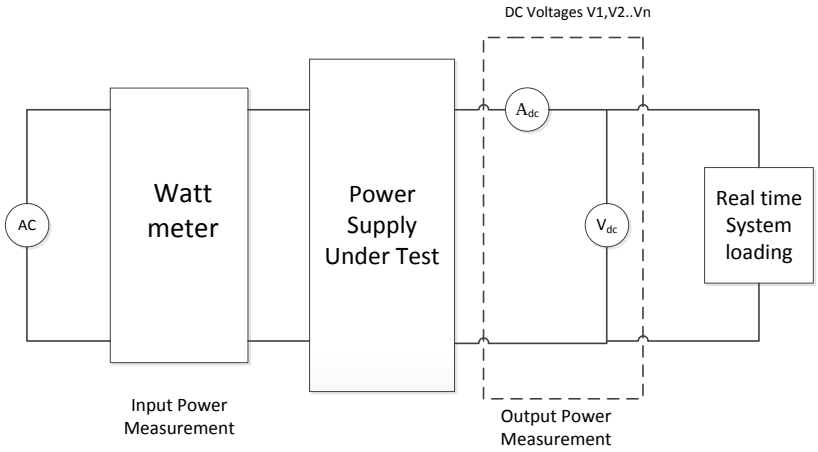


Figure 10: Real Time Energy and Efficiency Measurement Setup.

The wattmeter measures the input power while the output power is measured with ammeters and voltmeters on the output load side. In the case of multiple output systems such as the computers, multiple ammeters and voltmeters are required to measure the output power. For a particular loading condition, the efficiency of the power supply is calculated as

$$\eta = \frac{\text{Output Power}}{\text{Input Power}}$$

However, the main difference between conventional efficiency measurements techniques and this method is that in this case the efficiency of the power supply is measured while it is in real time operation rather than under laboratory conditions. This method of testing helps in computing the operational efficiency of the power supply rather than a worst case or best case efficiency. As it will be shown later in this chapter, the computer loads are extremely varying and hence the operating point changes within milliseconds. Hence to measure the efficiency accurately under real time loads, the measuring instruments should have data logging capabilities to record the measurements so that the input and output power measurements can be synchronized with each other and the efficiency measured over a wide range of operating points.

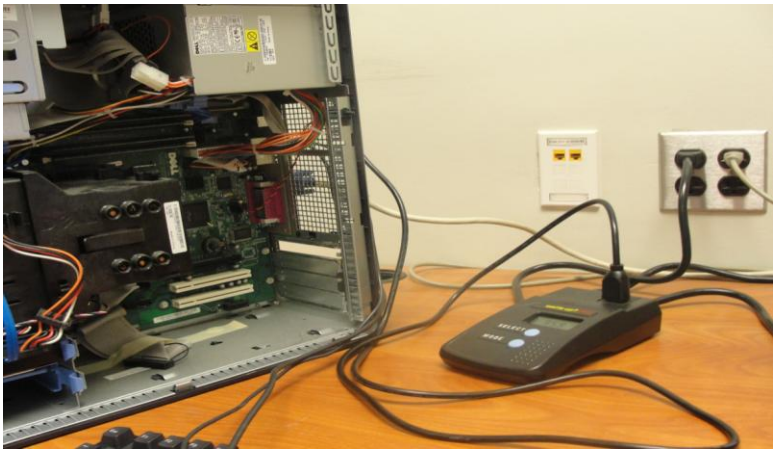


Figure 11: Watts up Meter Monitoring the ac Input Power of Desktop Computers.

A watts-up meter is used in this experiment to measure the input power and also record the measurements for a considerable amount of time (Capability- Nine hours of measurement with a resolution of one second). A picture of the meter in action is shown above in Figure 11.

To measure the output power, it is sufficient to measure the output current since the output voltage is fixed and has stringent regulation bands within which they operate. Measuring the output current for the computer power supplies is not very intuitive since there are multiple outputs coming out from computer power supply and the space existing for monitoring the dc output non-intrusively is extremely limited. In this experiment, two or three clamp-on dc current measurement sensors (as much as the space constraint permits) coupled with data loggers are used to monitor the dc outputs for a fixed period of time for a typical operating cycle (loading) and this process is repeated for the same operating cycle and power supply till all the dc output data have been captured.

However the typical operating profile for a PC load has to be defined so that it can be used not only to standardize the output current measuring process (for multiple output systems) but also to compare the energy consumed by different power supplies over a day. To define the operating cycle, initially 5-10 commonly used PC software application tasks like web browsing or running a video were defined and the input and outputs of the power supplies were monitored to analyze the effect of the different applications on the operational efficiency of the power supply. Another advantage of defining a typical operating cycle is that it helps in computing the amount of energy that is being lost in the power supply on a typical operating day and by computing this loss for the same operating cycle for different power supplies, the relative energy loss difference for the different power supplies can be quantified. It provides vital information about the margin there is for energy savings through power supply design improvement.

A typical PC operating load cycle has been defined and run manually. The operating cycle consists of usage of internet based applications (browsing, mailing, web

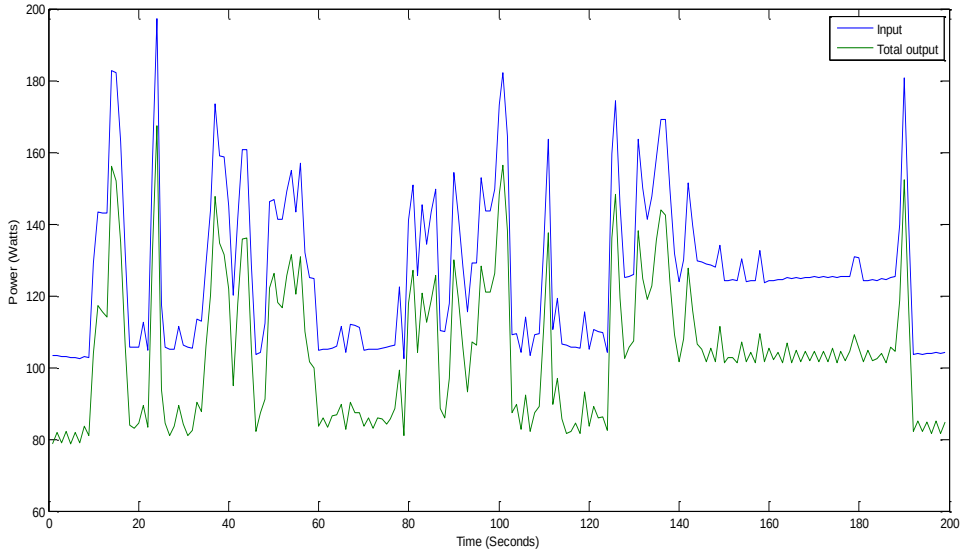
videos and games) for three minutes. This specific application was chosen since it provides a controllable mix of loads from idling (doing no active work), basic light level loading (checking mails, browsing) to extremely high loading (watching HD web streaming video) of the power supply and is also easily replicable.

In the measurement of the dc outputs to log the current data, initially a sampling rate of one second was used and this caused inconsistencies between the input and output power measured (output power was greater than the input). A more in-depth analysis of the data showed that one of the power supply outputs (12V) was changing extremely quickly (faster than 1 second) and hence the sampling rate of 1sample/sec used to log the data was not high enough for this output and so the input and output power measurements obtained were not synchronized. This was the cause of the inconsistencies. The frequency of output variation was so high that with 1 sample/sec sampling rate, the data recorded was instantaneous sample data (at random points over one second time period) and not the averaged value per second. So, all the dc outputs (5V, 3.3V, -5V and -12V) other than the 12V output were measured and logged using the current clamps and data loggers (one sample per second) whereas the data from the 12V output was logged using a Tektronix Digital Oscilloscope at a sample speed of 40,000 samples per second.

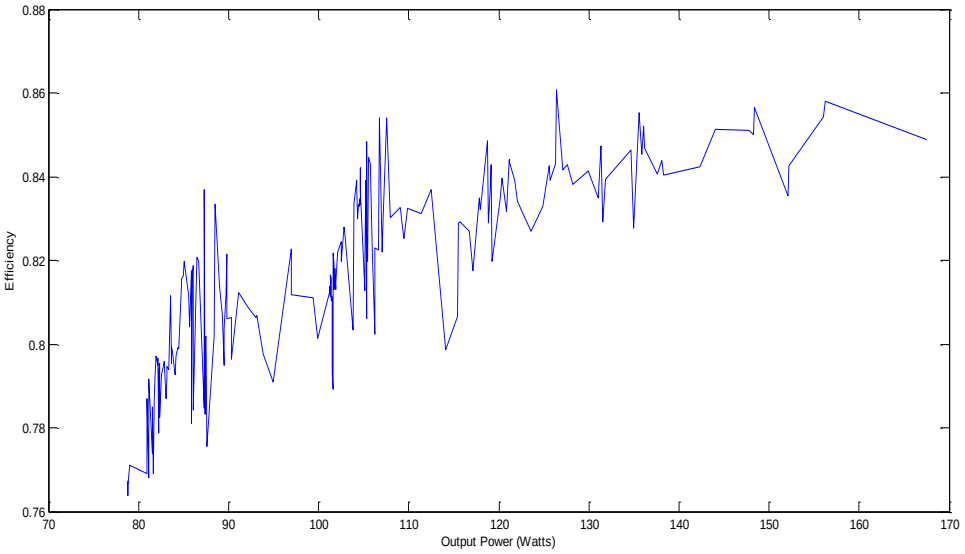
Using this measurement setup and the defined operating cycle, three power supplies were tested. The power supplies were carefully chosen so that they represented a good mix of the devices that exist in the market today (from low end to high end). The configuration of the computer system used to load the power supply was an Intel Pentium D 82945G processor with 3GB DDR2 RAM, 80 GB Hard drive, 256MB RAM NVidia Graphics card and a DVD-CD-RW. The graphs showing the input and output characteristics for two of the power supplies is shown below in Figures 12 and 13:

Power Supply 1: Diablotek DA 350W Power Supply (Cost: $20)

PC loading: Usage of Internet based Applications for three minutes (23 – 49% of full load).



(a)

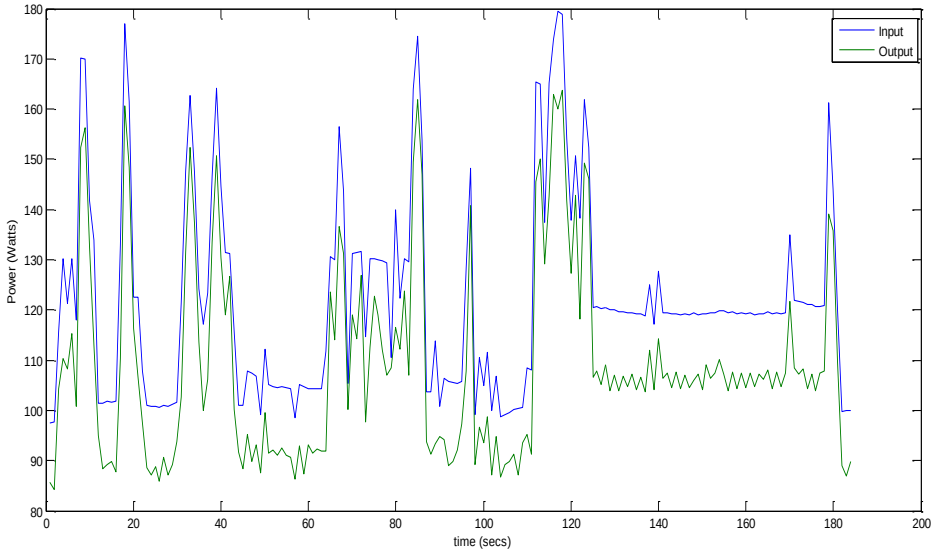


(b)

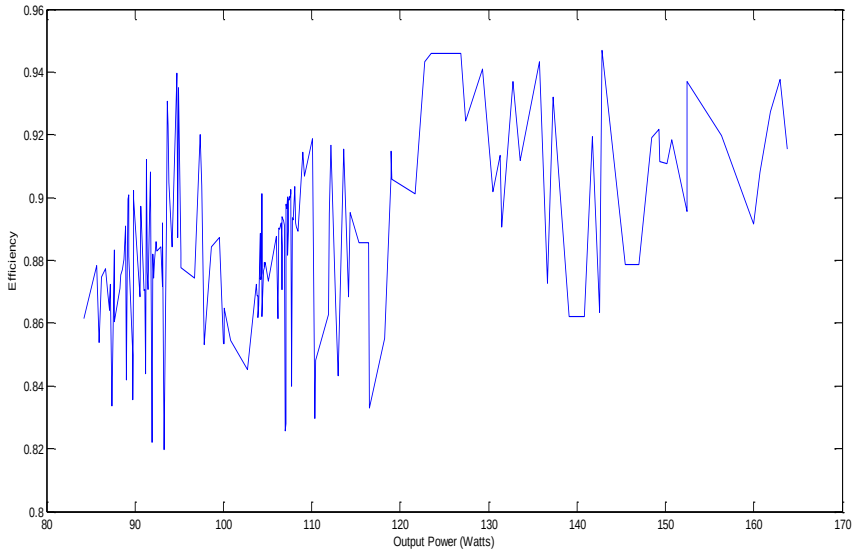
Figure 12: Characteristics of the Diablotek Power Supply (a) Input and Output Power vs. Time Curve (b) Efficiency vs. Output Power Curve

Power Supply 2: Antec –Basiq– 350 W Power Supply (Cost: $30)

PC loading: Usage of Internet based Applications for three minutes (24 – 47% of full load)



(a)



(b)

Figure 13: Characteristics of the Antec Power Supply (a) Input and Output Power vs. Time Curve (b) Efficiency vs. Output Power Curve

The average and idle mode efficiency and the input power factors for the three tested power supplies are shown below in Table 1.

Table 1: Summary of Test Results for the three Computer Power Supplies

	Diablotek-350W	Antec – Basiq 350W	Thermaltake Lite Power
Idle Mode Efficiency	74.5%	80.2%	85.9%
Average Efficiency	77.5%	82.5%	88%
Input Power Factor	0.55-0.6	0.58-0.64	0.96-0.99

3.2 Existing Energy Star 80 plus Efficiency standards

The Testing protocol of the Energy Star Program [3] recommends measuring the efficiency of the power supply under test at 20, 50 and 100 percent of full load output. They recommend a proportional allocation method for providing consistent loading guidelines for multiple output internal dc-dc power supplies i.e. 20% loading means each of the outputs are loaded to 20% of their full load output value (e.g. a 5V, 20A output is loaded to 4A). Derating is applied in cases where the sum of individually maximum outputs exceeds the total rated output of the power supply. However the results from the above experiments show that under normal operation of the personal computers most of the power is being consumed by the 12V output of the power supply. Almost 75% of the load is consumed by it while the rest 25% is shared between the 5V (20%), 3.3V (< 5%) and -12V (<1%) outputs. So 20% loading in this case is not 20% by proportional allocation but 20% load as consumed by the personal computer itself. The efficiency measurement results obtained by following the Energy Star Program recommended methods do not correlate with the results obtained and tabulated in Table 1 nor do they represent the actual operating efficiency of the power supply.

3.3. Energy Usage Projections per annum

To access the impact of energy lost in the different power supplies on a nationwide scale it is necessary to calculate the energy use and waste projections from both households as well as commercial applications.

3.3.1 Energy Consumption Projections for Households

The data from [30] suggests that globally, in an average household the computer is used 23 days a month on average. During this time, it is powered on for 7 hours and 34 minutes of which it is used effectively only for 2 hours and 51 minutes. The data also suggests that 63% of time spent by the user is on internet usage. The energy usage projections are computed by approximating (the other applications or loads also have an approximately similar profile as the internet usage profile) the entire effective usage time of the user to their internet usage. The energy usage and waste computations and projections for power supply 1 (Diablotek) during active mode of operation is shown below. The computations are performed by using the data from Figure 12 (a).

Energy spent during three minutes of active usage = 8.34 Watt-hours
Energy wasted during three minutes of active usage = 1.86 Watt-hours.

Approximate Projection of Energy spent per year = 5.7 kWh
Approximate Projection of Energy wasted per year = 1.27 kWh

The energy usage and waste projections during the power supply's idle mode of operation are shown below. Idle mode of operation for the computers is defined as the time during which the processor of the computer is doing no active work [31].

Time spent idling in a year = (7h 34mins – 2h 51mins) × 12 = 56 hrs and 36min

Energy spent in idling time = 113.8 × 56.6 = 6.44 kWh

Energy wasted during idling = (113.8 – 85.3) × 56.6 = 1.61 kWh

This computation is performed for the other two power supplies and the calculations are shown in Appendix A. Table 2 below shows the energy usage and waste projections for all the three power supplies for the household application. The projections are extremely conservative.

Table 2: Energy Waste Projections for Computer Power Supplies

	Diablotek-350W	Antec – Basiq 350W	Thermaltake Lite Power
Energy wasted idling (kWh/year)	1.61	1.21	0.76
Energy wasted in active mode(kWh/year)	1.27	0.92	0.58

Assuming that 60% of the US population has access to computers and 25 % of them use the computers regularly and if the energy wasted in the high end power supply (power supply 3- thermal take) is considered, then the amount of energy wasted in power supplies per annum in US households in idle mode is approximately 34GWh/year.

3.3.2 Energy Consumption Projections for Offices

The results of a survey [31] conducted on the time spent by computers in office spaces in the US under various power modes are presented below in Table 3

Table 3: Time Spent by Computers under Various Power Modes

	Hours per day spent in Sleep	Hours per day spent in Idle Mode	Hours per day spent in active mode
Without Power Management	0.0	23.3	0.7
With Power Management	16.0	7.3	0.7

Energy Waste Projections for three different power supplies computed using data from Table 3 are given below:

Table 4: Energy Waste Projections for Computer Power Supplies

	Diablotek-350W		Antec – Basiq 350W		Thermaltake Lite Power	
	Energy wasted idling (kWh/year)	Energy wasted in active mode(kWh/year)	Energy wasted idling (kWh/year)	Energy wasted in active mode(kWh/year)	Energy wasted idling (kWh/year)	Energy wasted in active mode(kWh/year)
Without Power management	242.37	9.51	181.4	6.89	114	4.35
With Power Management	75.94	9.51	56.83	6.89	35.73	4.35

From the results of Table 4 it can be seen that a considerable amount of energy is being wasted in these power supplies especially during their idle mode of operation. Even assuming a modest number of 10 million office computers, the amount of energy wasted in the high end power supplies with power management turned on is 350GWh/year in the idle mode of operation alone.

These results clearly indicate that there exists a staggering potential to improve the efficiency of the computer power supply at both the household as well as the office level and that even one-watt of energy saved would have a tremendous impact on the system wide scale.

3.4. Summary

The first part of this chapter proposes a new method to measure and quantify the efficiency of the computer power supplies under real time loading conditions. The second half of the chapter analyses the data from the efficiency logging and measurements to project the energy usage and waste (per annum) in the computer power supplies at both the household and the commercial level on a nationwide scale. The results obtained from this chapter clearly show that there exists a potential to improve the efficiency of the power supplies. The next chapter provides a similar analysis and makes a case for the printer power supplies.

CHAPTER 4

TESTING OF PRINTERS AND ESTIMATING THEIR ENERGY CONSUMPTION

Other than computers, many other electronic loads like printers, microwaves, LCD Televisions, cell phone chargers also show wide range in average to peak power use. It is likely that the power supplies in these devices were designed for maximum power delivery point, and may have poor efficiency at lower power levels. It is important to research potential for energy use reduction through power supply redesign for these high penetration electronic loads. In pursuit of this goal the above stated applications were tested and it was found that other than for the printers, the light load energy consumption of the rest of appliances was extremely low. Hence in this chapter, the results from the testing of various printers ranging from household use to commercial multifunction printers are detailed and their energy consumption is projected to see if there is a potential for energy consumption reduction.

4.1 Market Research

The data from [32] suggests that in the second quarter of 2010 alone the sales of printers worldwide amounted to 29 million units and the US alone accounting for 6.5 million units of sales. The Laser segment accounted for 27% of the market share or 7.8 million units [32]. Multi functional printers (MFPs) took up 62% share in the laser segment or 4.8 million units [32]. This data suggests that the printer market is huge with sales of commercial grade MFPs in the US alone amounting to 1 million units and the basic MFPs 3.3 million units.

4.2 Energy Consumption of Printers

With such a large market share, even one watt of continuous energy wastage in these printers amounts to 226GWh of energy loss per year in the US (in the newly sold printers). This data suggests that there may be a potential for energy consumption reduction in the printers. However a wide variety of sample data from testing different types of printers is required to justify the cause. So, the energy consumption of one basic laser jet printer and three commercial grade multifunctional laser jet printers were monitored. The results from the tests are detailed in sections 4.2.1 and 4.2.2

4.2.1 Energy consumption and projection of basic laser jet printer

A HP Laser Jet 4250 printer (printer 1) was tested to determine the amount of energy consumed by this printer under various load cycles. The power consumption cycle of the HP laser jet 4250 printer for printing a single sheet of paper is shown in Figure 14.

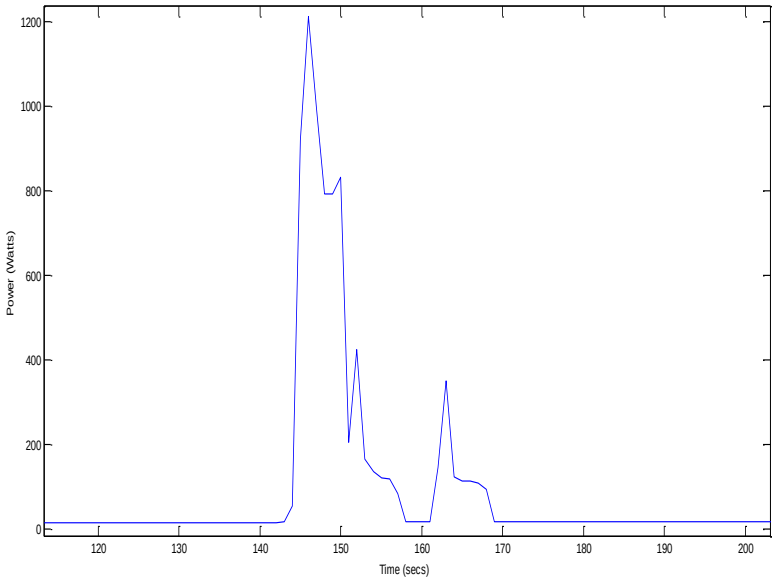


Figure 14: Power Consumption Cycle of a Printer for Printing One Sheet of Paper

In its idle state the power consumed by this printer is 17W.To measure the amount of energy consumed by the printer for actively printing different quantities of paper, the energy consumed by the printer for printing 1,2,3,4,5 and 10 sheets of papers were measured. The results of the experiment are shown below in Table 5 and Figure 15.

Table 5: Energy Consumed by Printer 1 for Printing Different Quantities of Paper

Sheets of Paper printed	1	2	3	4	5	10
Energy Consumed (Watt hours)	2.23	2.45	2.78	3.18	3.50	5.11

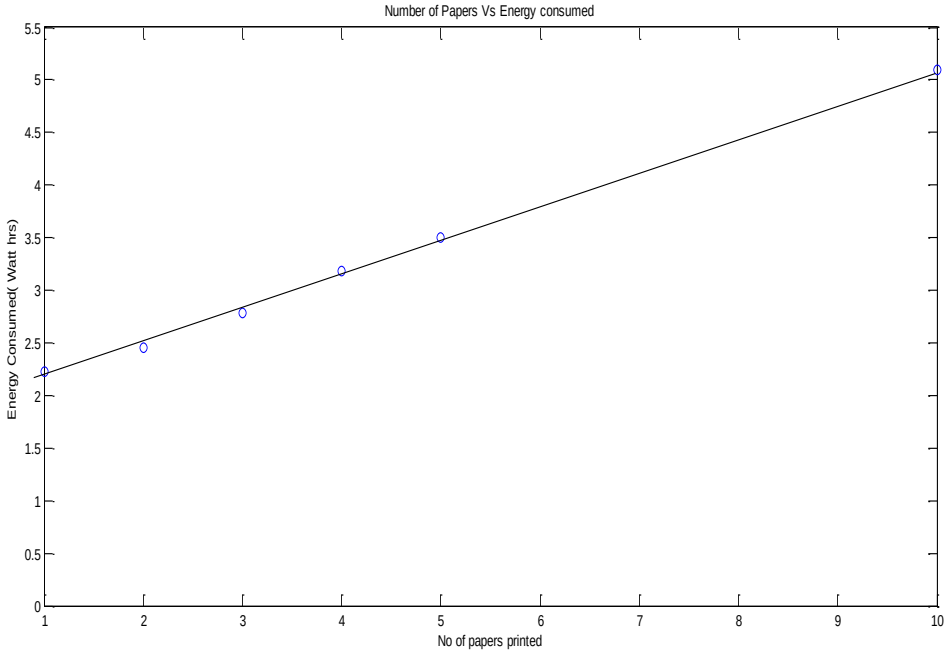


Figure 15: Plot showing the Energy Consumed by Printer 1 for Printing Different Quantities of Paper

Printing the first sheet of paper consumes 2.23 Watt-hours of energy and for every additional sheet approximately 0.22 to 0.32 Watt-hours is consumed. The response is almost linear and hence from the above data the amount of energy this printer will consume for printing any arbitrary number of sheets of paper can be predicted. The power and energy consumption of the printer 1 under different modes of operation have been tabulated in Tables 6 and 7. The idle mode, standby mode and the energy saver modes of operation for the printer are explained in section 4.2.2.

Table 6: Power Consumed by Basic Laser Jet Printer in Idle Mode of Operation

	HP Laser jet 4250
Power Consumed in the Standby Mode	19W
Power Consumed in the Energy Saver Mode	17W

Table 7: Energy Consumed by Basic Laser Jet Printer while Printing

	HP Laser jet 4250
Energy Consumed to print a single sheet of paper	2.23Wh
Energy Consumed to print every next sheet of paper.	0.23-0.32Wh

4.2.1.1 Energy Usage Projections (per annum)

To compute the energy usage projections per annum for the given printer, the loading cycle of the printer 1 was monitored on a busy weekday. The results of the experiment are shown below in Figure 16.

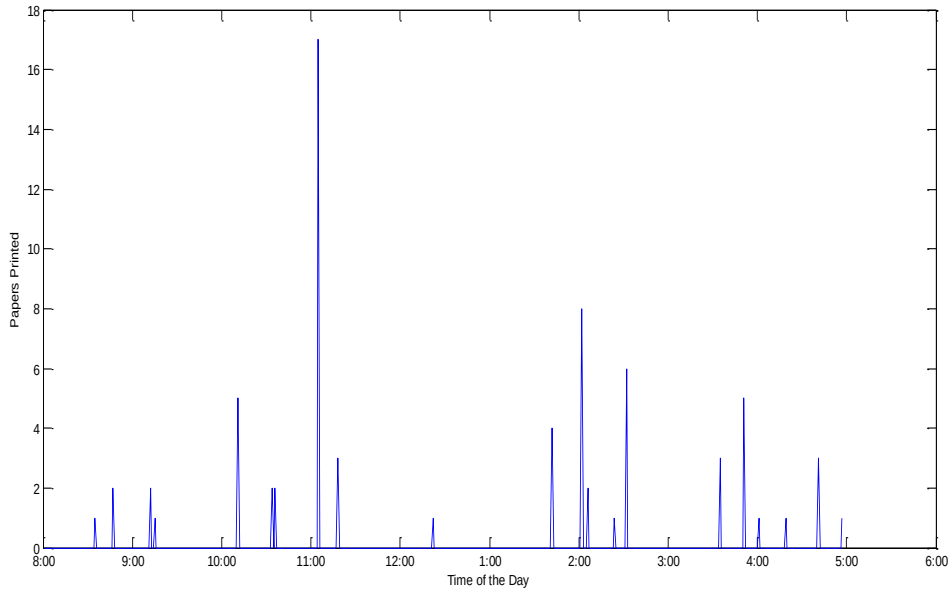


Figure 16: Load Cycle of HP Laser Jet 4250 Printer for One Day.

It has been assumed that the printer is used actively for five days of the week, fifty two weeks of the year and that the above mentioned printer daily load cycle is the same throughout the year.

The energy consumed by the printer in a day in its active mode is 62.8 Watt-Hours (This is obtained from the load cycle shown in Figure 16) and the energy consumed by the printer in a day in its idle mode is 408 Watt-Hours (= 17W × 24 hours). The projected energy consumed by the printer in a year is computed and the results are shown in Table 8.

Table 8: The Projected Energy Consumed by the Printer 1 (per annum)

Mode of operation	Energy Consumed per year	Energy Consumed by 13.2 Million units of the basic MFPs
Active Mode (used 5 days of the week)	16.3kWh	216GWh
Idle Mode (used 7 days of the week)	149 kWh	1964GWh

From the results shown in Table 8 it can be clearly seen that the amount of energy consumed by the basic laser jet printer is substantially more in the idle mode of operation than when the printer is being actively used (for this particular load cycle).

4.2.2 Energy consumption and projection of commercial Grade MFPs.

The energy consumed by three commercial grade multi functional printers under different modes of operation was measured using the watts-up power meter. The power and energy consumed by the Ricoh-Atcio MP4000 Laser Jet printer over a 10 minutes period of time is shown in Figure 17.

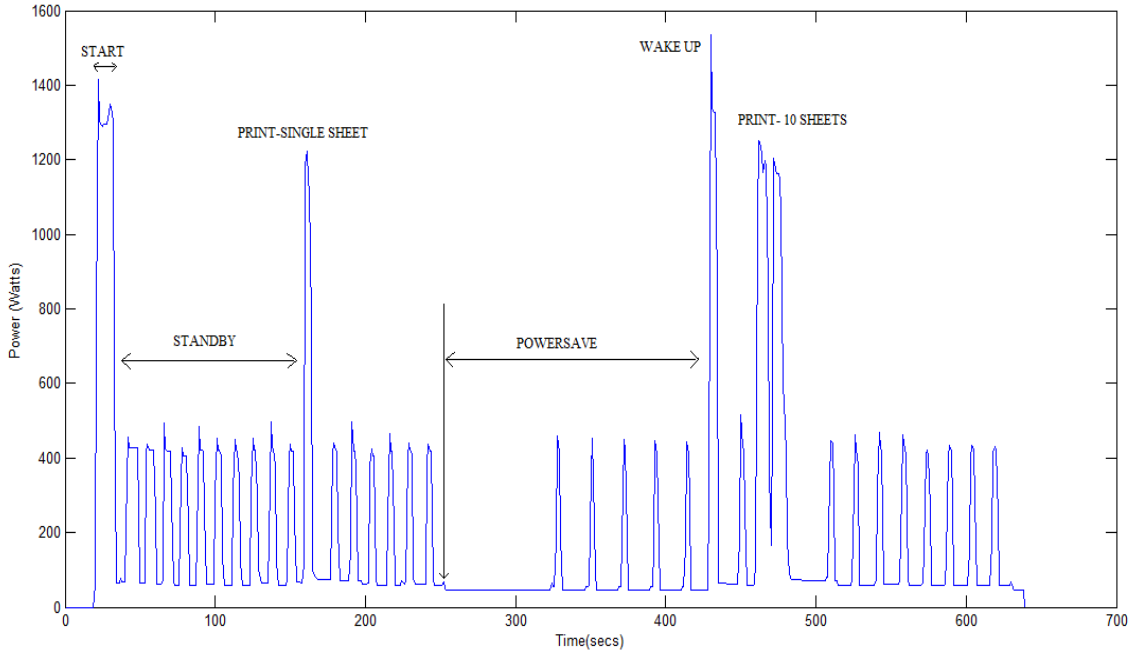


Figure 17: Power and Energy Consumed by Ricoh-Atcio-MP 4000 Laser Jet MFP under Different Modes of Operation.

When a printer is doing active work such as printing, it is defined to be in its active mode of operation. From Figure 17 it can be seen that even when the printer is not printing and is in its standby mode of operation, power is still being consumed by it. This is because, during the standby mode the printer consumes energy every few seconds to maintain the temperature of its fuser (it is a component which is essential to printing. If the fuser were not maintained at a particular temperature, when the print command is given, it would take some time for the printer to heat up the fuser before starting to print.) The energy saver mode in this printer saves energy by maintaining the fuser at a lower temperature than in the standby mode (hence consumes lesser energy). The definition of energy saver mode and the standby mode may vary from printer to printer since in some new models, the printers use instant on fuser whereby the standby and energy saver modes do not have to maintain the fuser at a particular temperature and hence the energy

consumed during these modes is lower. However the common factor in all the printers is that during the standby mode and energy saver mode of operations the printer is not doing any useful work and consumes significantly lesser power than in their active modes. So broadly the modes of operation of a printer can be classified into active mode operation and idle mode operation (standby and energy save modes).

The power and energy consumed by the three tested commercial grade MFPs under different modes of operation are shown in Tables 9 and 10.

Table 9: Power Consumed by Commercial Grade MFPs in Idle Mode

	Ricoh-Atcio-MP4000	Konica Minolta – Bizhub-420	Oce im3512
Power Consumed in the Standby Mode	145 W	180-185W	185-190W
Power Consumed in the Energy Saver Mode	95W	56.6W	66.5W

Table 10: Energy Consumed by Commercial Grade MFPs while Printing

	Ricoh-Atcio-MP4000	Konica Minolta – Bizhub-420	Oce im3512
Energy Consumed to print a single sheet of paper	1.65Wh (600W Average)	1.42Wh (640W Average)	1.76Wh (630W Average)
Energy Consumed to print a single sheet of paper. (double sided printing)	2.48Wh (550W Average)	2.19Wh (650W Average)	2.94Wh (660W Average)

4.2.2.1 Energy Usage Projections (per annum in US):

To estimate the energy consumed by these printers over a period of a year, the printers have been assumed to operate on a very heavy duty cycle of printing a hundred thousand sheets per year. The estimated energy usage calculations are shown for the Ricoh-Atcio-MP4000 laser jet printers. To estimate worst case scenarios each print is assumed to be in cycles of 10 pages. The energy and time consumed for printing 10 sheets of paper in this printer has been experimentally computed to be 6.57Wh and 20 seconds respectively. The printer is assumed to be in power save mode for 16hrs a day and in standby mode for 8hrs a day (i.e. when not in active operation).

The energy consumed for printing one hundred thousand sheets per year is 65.7kWh (=10000sets of 10sheets × 6.57Wh/10sheets). The time consumed for printing one hundred thousand sheets is approximately equivalent to 3 days (= 20secs × 10000 / (3600 × 24)) of continuous usage of the printer. Then the energy consumed by this printer in its idle mode per year is 973kWh per year (= (95Wh×16hours/day + 145Wh×8hours/day) × (365-3) days).

The energy projection computations are performed similarly for the other two MFPs and the results are shown in Table 11.

Table 11: Energy Usage Projections for Commercial Grade MFPs per annum

	Energy Consumed per annum (kWh)		
	Ricoh-Atcio-MP4000	Konica Minolta – Bizhub-420	Oce im3512
Active Mode (100000 sheets per year)	65.7	55	71
Idle Mode	973	850	935

To calculate the overall energy consumption in the commercial grade printers sector, the total sales of 4 million units in this sector (from section 4.1, sales of 1 million per quarter in this sector) are assumed to be distributed equally among the 3 tested MFPs. Then the energy that is consumed by four million units of the commercial grade MFPs per year in active mode is 256GWh (= (65.7 + 55 + 71) kWh × 4millionunits × 0.333). The energy consumed by 4 million units of commercial grade MFPs per year in idle mode is 3,680GWh.

It can be clearly seen that the energy being consumed even in the worst case biasing (towards active mode) is higher in the idle mode of operation. From the results obtained in sections 4.2.1.1 and 4.2.2.1, it can be seen that there clearly exists a potential to reduce the energy being consumed by these printers in their idle mode of operation.

4.3 Summary

In the first part of the chapter, the amount of sales for the different types of printers in the US was documented. A high level approach was taken in order to access the energy consumed by the basic and MFP printers under their active and idle modes of operation. The data and results presented through this chapter have clearly established that the amount of energy wasted in the printers at both the household and commercial levels are substantial especially in their idle mode of operation. Hence there exists a serious potential to redesign the power supply used in these printers and reduce the energy losses tremendously on a nationwide scale. The next chapter addresses the question of where the energy is being lost in these power supplies and how they can be minimized.

CHAPTER 5

PROBLEM INDENTIFICATION, STATEMENT AND PROPOSED SOLUTION

5.1 Problem Identification

The results from chapters 3 and 4 suggests that there is a considerable amount of power being consumed and wasted in the printer and desktop computer power supplies. Hence it has been established that there does exist potential for redesigning the power supply for better efficiency. However, to redesign the power supply it is necessary to find out in which elements of the power supply the energy is being lost, whether the losses are concentrated or distributed and how cost effectively can these losses be removed. To find out the lossy elements in the power supply, the mid-cost range Antec 350W power supply was broken down and the circuit was removed from its housing. From the circuit board, the circuit of the power supply was retraced. The circuit schematic of the power stage of this power supply is shown in Figure 18.

To find the components or parts of the circuit in which most of the energy is wasted, the circuit schematic of the power stage of the Antec-350W power supply was simulated using MATLAB in open loop mode. The simulation results were then used for the computation of losses. The losses were computed for three operating points of the power supply ranging from idle mode (mode 1), mid-scale output (mode 2) and peak output conditions (mode 3). The detailed loss calculation using the simulation results are shown in Appendix B. The losses in the various elements of the power supply under those three modes of operation are shown in Table 12.

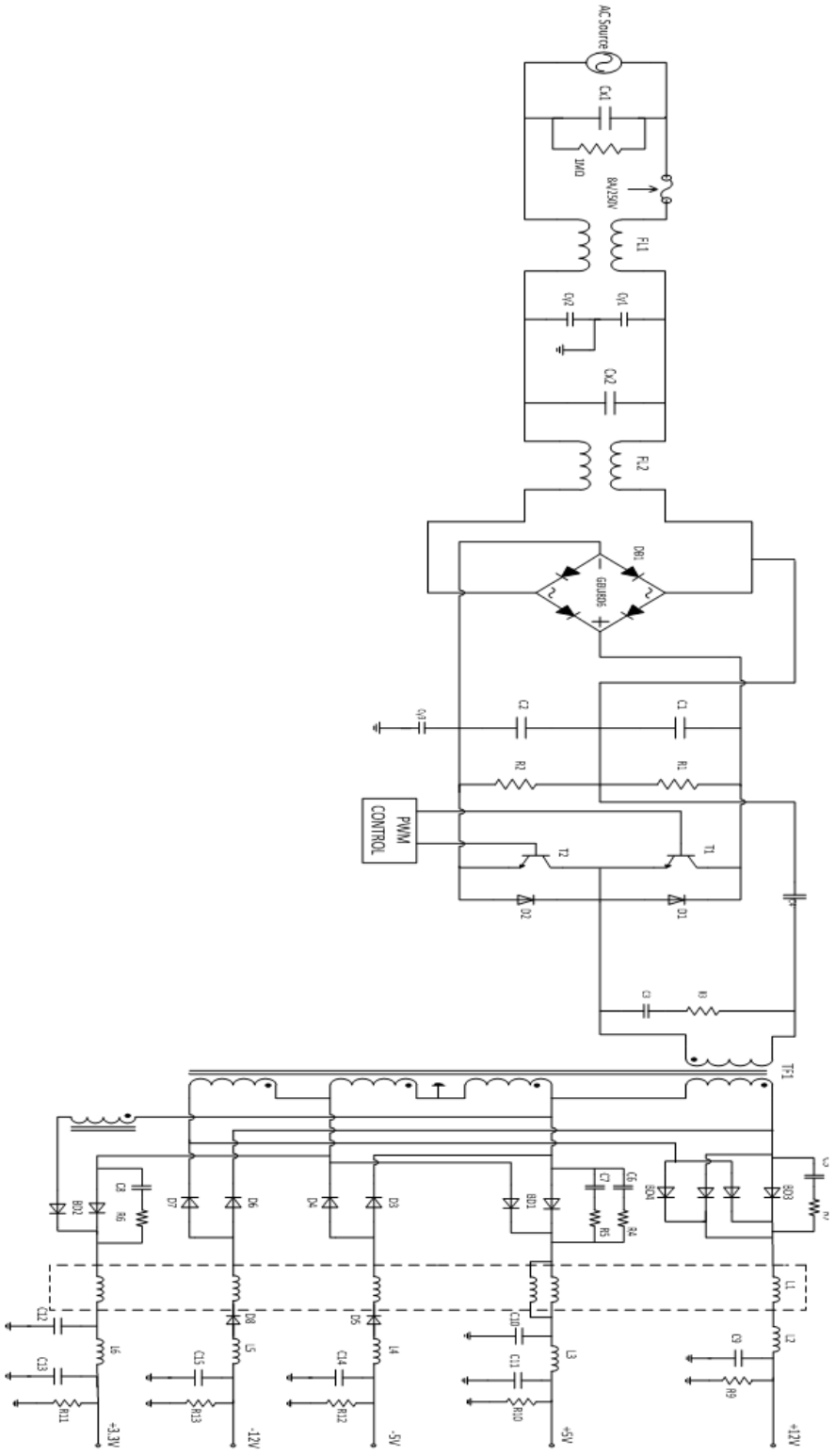


Figure 18: Schematic of the Power Stage of Antec –350W Computer Power Supply.

Table 12: Losses in Various Elements of the Power Supply under three Modes of Operation

S. No	Lossy elements	Mode of Operation - 1	Mode of Operation - 2	Mode of Operation - 3
1	**Input Diode Bridge**	0.5W	0.86W	1.16W
2	**Input Power Switches (Conduction)**	0.9W	1.56W	2.1W
3	**Input Power Switches (Switching)**	2.4W	4.2W	5.66W
4	**Output diode Rectifiers**	8.79W	13.29W	15.86W
5	**Resistances**	4.2W	4.2W	4.2W
6	**Cooling Fan**	2W	2W	2W
	Total Estimated Loss	18.8W	26.1W	31W
	Actual Loss	20.1W	27W	33W

The losses in the power supply under study have been classified into 6 major areas. The first three areas belong to the input side circuit of the power supply and are fairly distributed. The losses in the resistances and cooling fan are due to extremely cheap

and careless design and can be easily eliminated by using simple design changes or better control methods and most power supplies eliminate this loss. However a major portion of the losses is concentrated in area 4 (Diode rectifier). Since the computer and printers present a low voltage high current load, the losses in the diode rectifier are further exaggerated. The next section defines the problem statement for this research work taking into account the results from Table 12.

5.2 Problem Statement

The aim of this research work is to identify/develop cost effective, mass scalable yet high impact solutions to allow improved matching of the load requirements, as well as minimization of the energy consumption in the power supply over the defined operating cycles. The solution should be minimally intrusive and easily adaptable to the existing circuits without much design overhead. One of the most important objectives is that the solution should be applicable universally i.e. power converter topology independent. The analysis performed and the results shown in Chapters 3 through 4 clearly shows that the losses in the standby mode of operation of the devices employing the power supply far exceed the losses during the active mode of operation as the device spends most of its time in standby or sleep or idle mode of operation. Hence the solution should cost effectively improve the efficiency of the power supply during its idle or standby mode of operation i.e. under light load conditions.

5.3 Proposed Solution

The results of Table 12 and the analysis performed in section 5.1 shows that the diode rectifiers are the biggest contributors to the energy loss in the power converter. A solution which targets elimination of this loss would definitely be high impact. Synchronous rectifiers can do this job effectively but would be too expensive if they are rated for the full load current. A two terminal device is proposed in this work, which can

be paralleled with the diode and controlled in such a way that under light loading conditions the synchronous rectifier operates and eliminates the rectifier loss whereas under high current mode of operation, the diode conducts and the circuit operates as if the synchronous rectifier was not there. In this way a low current synchronous MOSFET can be used which would decrease the cost of the proposed solution but would have maximum impact on energy consumed. The proposed device is completely self controlled and does not require external circuitry. All the sensing that is required to control the synchronous rectifier and to make it operate as a diode are all obtained from the voltage information across the two terminals of the device. This solution is minimally intrusive as it can be directly paralleled with the existing diode rectifier or in some cases even replaces the existing rectifier. No change of existing control circuitry, algorithms or design change of the power supply board layout is required. This solution is also topology independent as the two terminal device tries to emulate the diode operation exactly. Hence the proposed solution addresses all the challenges in the problem statement.

The two terminal device SSSR (Self Sufficient Synchronous rectifier) not only provides the logic to control the on-chip synchronous rectifier but also the control power to power the logic devices and to drive the synchronous rectifier. The basic block diagram of the proposed SSSR device is presented below in Figure 19.

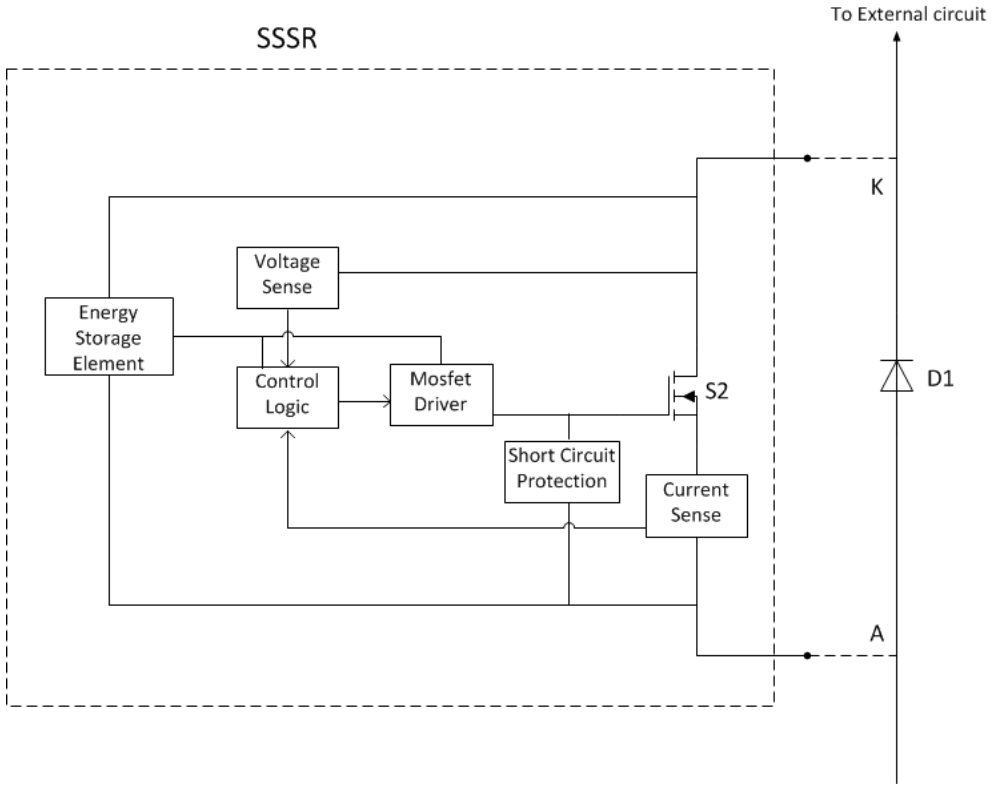


Figure 19: Block Diagram of the Proposed Two Terminal Self Sufficient Synchronous Rectifier (SSSR)

5.3.1 Operation

The SSSR is a two terminal device that tries to emulate the exact operation of the diode. The active element in the SSSR is a synchronous rectifier S2 which is controlled appropriately to mimic the operation of the diode. The device senses the voltage across the synchronous rectifier and the current through it to control the rectifier appropriately. When the primary switch is conducting, the voltage V_{AK} across the diode D1 and the SSSR is less than zero. The SSSR control senses this and prevents the synchronous switch S2 from turning ON for the entire period when the primary switch is ON. However during this period, the energy from the external circuit is stored in the energy storage element of the SSSR. This energy is used to power the control and drive circuits of the SSSR when the synchronous switch is turned ON. The block diagram of the SSSR under this mode of operation is shown in Figure 20.

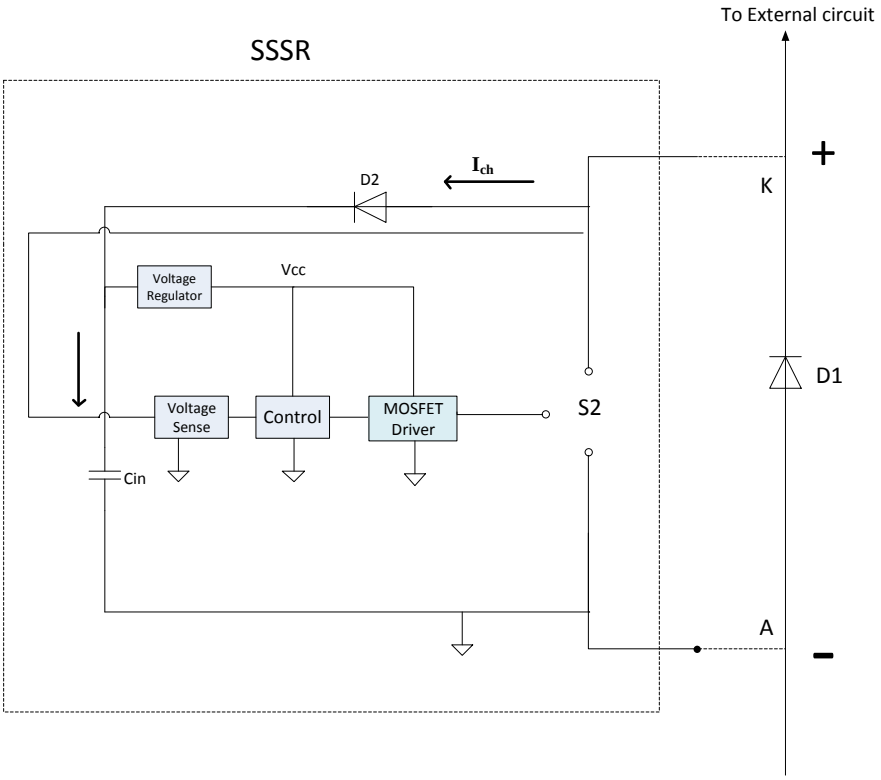
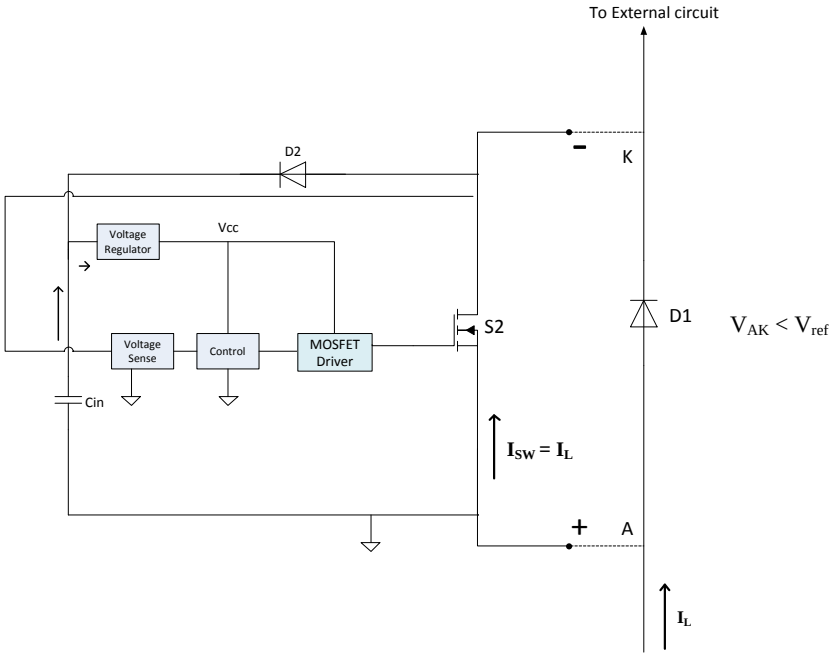
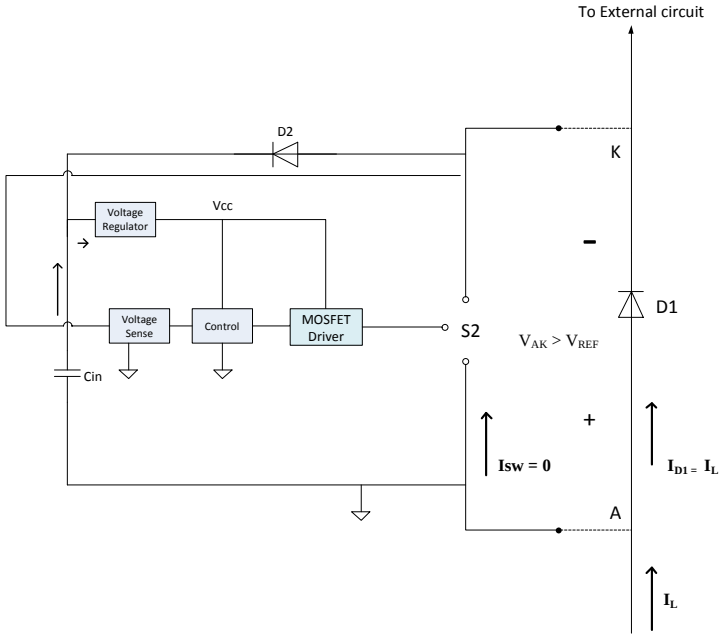


Figure 20: Operation of the SSSR when $V_{AK} < 0$.

During light load operation (when the power supply is operating in standby, idle or sleep modes) when the current through the device ($I_{SW} = I_{LOAD}$) is less than a reference current I_{REF} (or equivalently $V_{AK} < V_{REF}$, where $V_{REF} = I_{REF} \times R_{DS\,(ON)}$), the SSSR is turned ON and it operates instead of the diode D1 and hence removes almost all the losses across the otherwise lossy diode rectifier. However when the load current increases above I_{REF} , the SSSR turns off and lets the diode carry the load current. Now the circuit operates as if the SSSR were not present in the circuit and losses in the power supply remain the same as before (plus additional control power loss for the SSSR, which is very low). These two modes of operations are illustrated below in Figure 21 (a) and (b).



(a)



(b)

Figure 21: Block Diagram of the SSSR when $V_{AK} > 0$ (a) Light Load operation ($I_L < I_{REF}$)

(b) $I_L > I_{REF}$

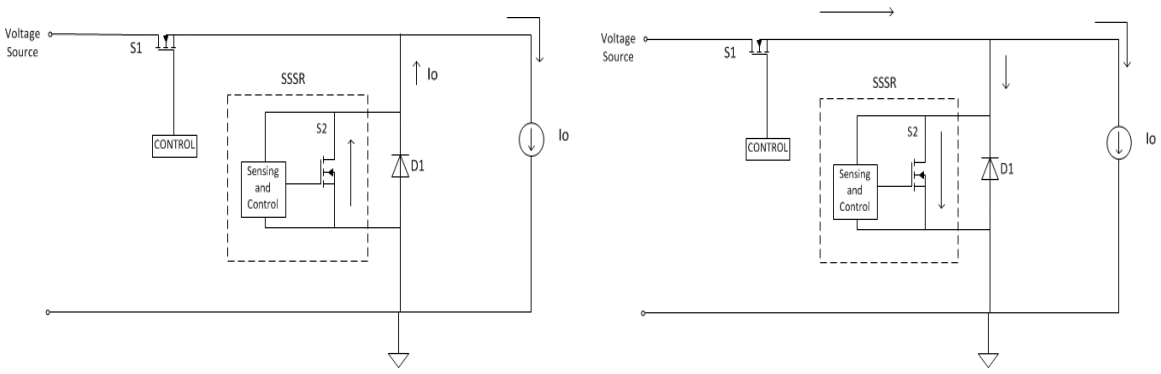
The control logic used to control the SSSR is summarized in the Table 13 below.

Table 13: Control Logic for the SSSR

S. No	Voltage across the device (V_{AK})	Load Current (I_L)	State of SSSR
1	$V_{AK} < 0$	Any	OFF
2	$V_{AK} > 0$	$I_L < I_{REF}$	ON
3	$V_{AK} > 0$	$I_L > I_{REF}$	OFF

5.3.1.1 Short Circuit Protection of the SSSR

The SSSR is equipped with a short circuit protection block to protect it and the external circuit from a potential short circuit. The need for short circuit protecting the SSSR is explained using a typical application circuit and is shown below in Figure 22 (a) and (b).

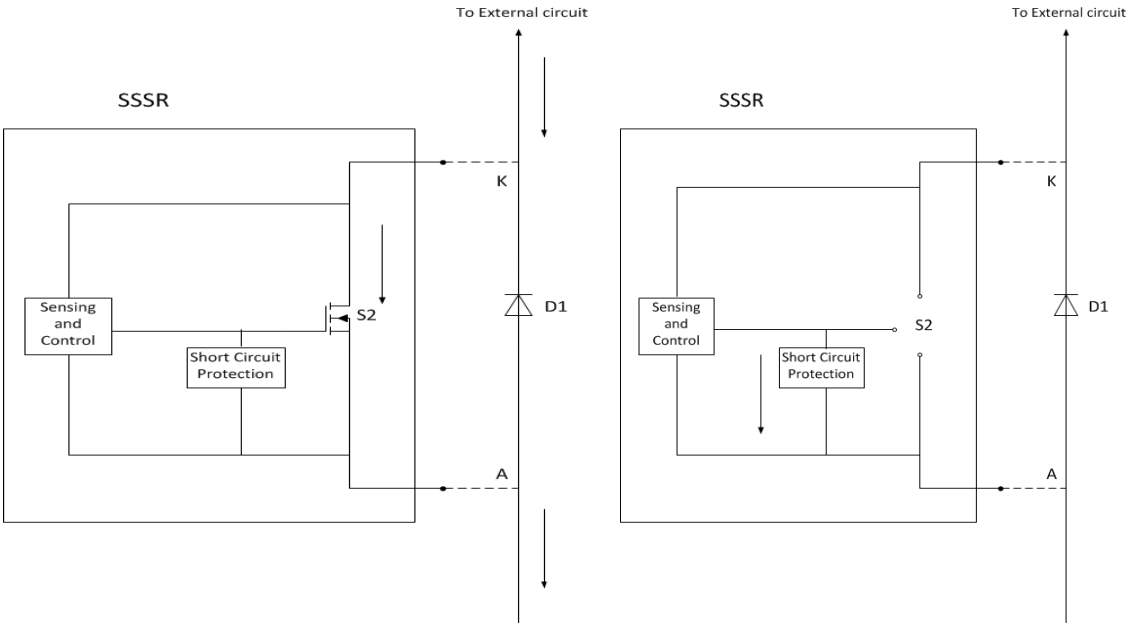


(a) (b)

Figure 22: (a) Application Circuit of the SSSR (b) Short Circuit caused due to Simultaneous Conduction of Both the Switches S1 and S2 (of SSSR)

The SSSR is used to replace the diode D1 as shown in the above circuit. If the SSSR ideally mimics the operation of the diode, then when the main switch S1 is turned ON, S2 of the SSSR has to immediately turn OFF and when S1 is turned OFF, the load

current has to automatically transition to S2. When S2 is conducting the load current instead of the diode and the main switch S1 is turned ON according to the control signals from its main controller, the synchronous switch S2 should ideally turn OFF immediately. However due to the delays associated with the sense and control circuits of the SSSR there is a time delay introduced between the turning ON of the switch S1 and the control pulse sent to turn OFF S2 and hence this causes simultaneous conduction of both the switches S1 and S2. This results in a short circuit of the input source as shown in Figure 22(b). This situation can be prevented by using a short circuit protection block which springs into action when it senses a short circuit. When the short circuit occurs due to simultaneous conduction of both the switches S1 and S2, the current starts rising through S2 in the reverse direction as shown in Figure 23 (a). This is sensed by the short circuit protection circuit which immediately shorts the gate of switch S2 thereby opening switch S2 and hence preventing the short circuit. This is shown in Figure 23 (b).

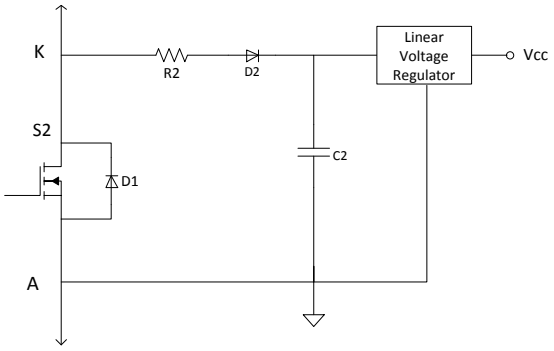


(a) (b)

Figure 23: (a) Short Circuit causes Current to Rise through Switch S2 (b) Short Circuit Protection Circuit in action.

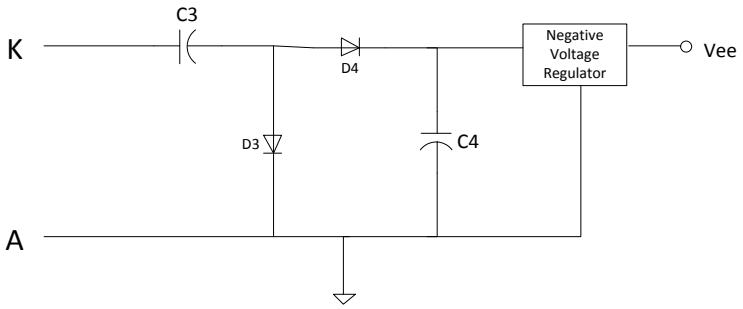
5.3.2 Proposed Circuit of the SSSR

The proposed circuit diagram of the SSSR is shown below in Figures 24 in parts. Figures 24(a) & (b) represent the power storage or reference voltage generating components of the SSSR. The Capacitor C2 in Figure 24 (a) charges through the R2 resistor when the voltage across the synchronous switch V_{AK} is less than zero. The size of the capacitor can be computed depending on the energy required for the control and drive circuits and the operating frequency of the power converter. The voltage across the capacitor is then regulated to V_{CC} using a linear voltage regulator to provide the stable voltage for the control logic elements and the drive circuit. Even though the linear voltage regulator has a very bad efficiency (efficiency is approximately Vo/Vin), the linear regulator provides a very simple and cost effective solution. So if the circuit is designed such that the gate and control power required are negligibly small, then even though the regulator has a bad efficiency the amount of energy wasted in it can be neglected. The switch S2 has to be chosen such that the gate power required for its turning ON and OFF is negligible. The gate power required for driving a MOSFET is directly proportional to its total gate charge Qg and hence by choosing a MOSFET with extremely low Qg (few nC) the gate power required and hence indirectly the loss in the regulator can be minimized.

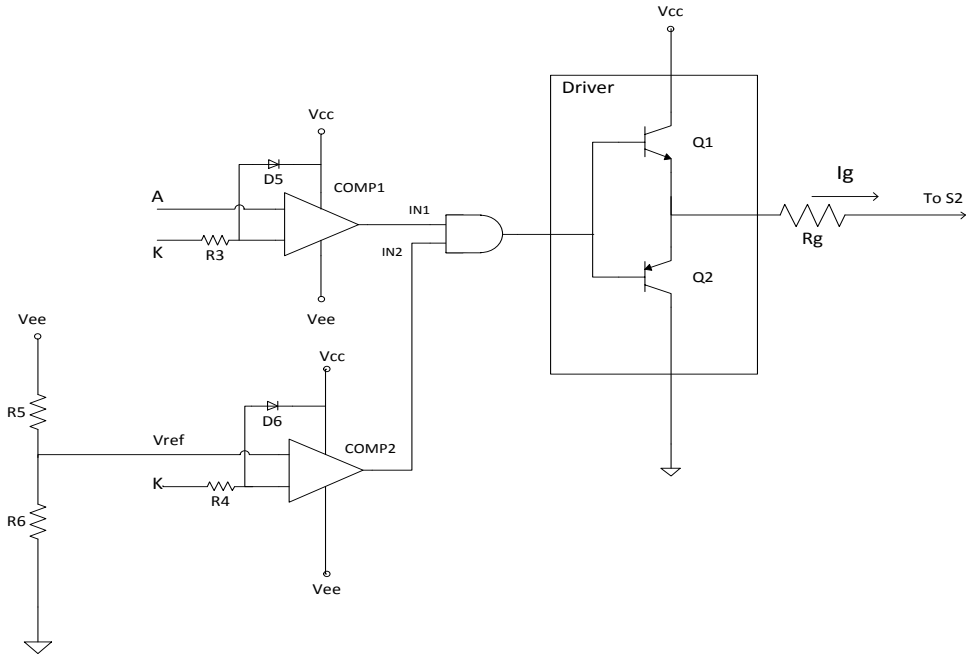


(a)

Figure 24: (a) Positive Reference Voltage Generator (b) Negative Reference Voltage Generator (c) Complete Drive and Control Circuit of the SSSR.



(b)



(c)

Figure 24 continued: (a) Positive Reference Voltage Generator (b) Negative Reference Voltage Generator (c) Complete Drive and Control Circuit of the SSSR.

The negative voltage reference generator is required for generating the negative reference (V_{REF}) for use in the current sensing comparator circuit shown in Figure 24 (c). Since the voltage V_{KA} is pulsating, a charge pump circuit as shown in Figure 24 (b) has been used to generate the negative reference voltage V_{ee}.

The circuit schematics of the control and drive blocks of the SSSR are shown in Figure 24 (c). The comparator 1 is used as the zero crossing detector. When the voltage

V_{AK} becomes greater than zero, the output of comp1 becomes high. If the current through the switch S2 is greater than I_{REF}, then the output of comparator 2 is low and hence the output of the AND gate and the corresponding MOSFET driver is low. This turns OFF the MOSFET for that switching cycle. However if the current through the switch is less than I_{REF}, the output of comp2 is high and hence the MOSFET is kept ON for that switching cycle.

The voltage V_{KA} is fed as the input to the comparators. Any over voltage across the input terminals of the comparator will damage it. Hence diodes D5 and D6 are used to provide input over-voltage protection to the comparators 1 and 2 respectively. When V_{KA} becomes greater than $V_{CC} + V_{f\,(D5)}$, the diode becomes forward biased and hence prevents the input to the comparator from rising above $V_{CC} + V_f$. Any over current is prevented by the resistors R3 and R4 respectively.

The circuitry involved in realizing the short circuit protection block is shown in Figure 25.

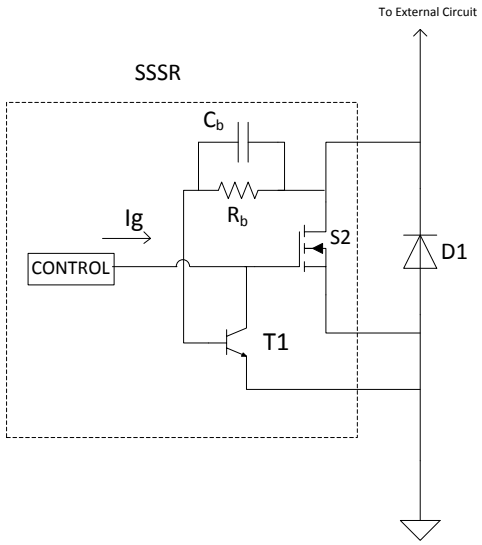
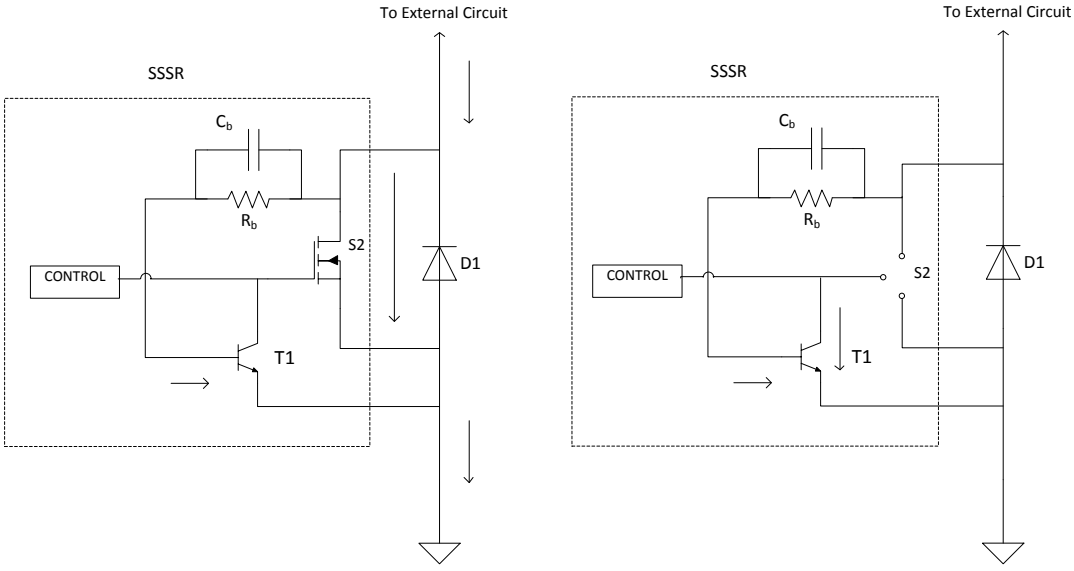


Figure 25: SSSR with Short Circuit Protection Circuitry.

The features of short circuit protection of the SSSR are realized by using a single transistor and a RC component. When S1 is turned ON, and the control signal to turn

OFF S2 has not yet reached the gate terminal of S2, a short circuit occurs, i.e. both S1 and S2 are conducting. This causes the current through S2 to rise quickly which in turn causes the voltage drop across the resistor R_b to increase above the biasing voltage of 0.6V of T1 as shown below in Figure 26 (a).



(a) (b)

Figure 26: (a) Current Rises through S2 due to a Short Circuit (b) Short Circuit Protection Block springs into action and Prevents the Short Circuit

Now transistor T1 turns ON immediately and hence shorts the gate of S2. This causes an immediate turn OFF of S2 and the diode D1 becomes reverse biased as usual. Within a few nanoseconds, the control pulse to turn OFF S2 reaches its gate terminal and this keeps S2 OFF and also turns OFF T1. Since T1 is ON only for a few nanoseconds, the loss in it is negligible

5.3.3 Test Bed

To initially test the SSSR, a test bed is required on which the SSSR can be implemented and its effectiveness proven. A simple buck converter is used here as the test bed. The circuit diagram of the buck converter is shown below in Figure 27.

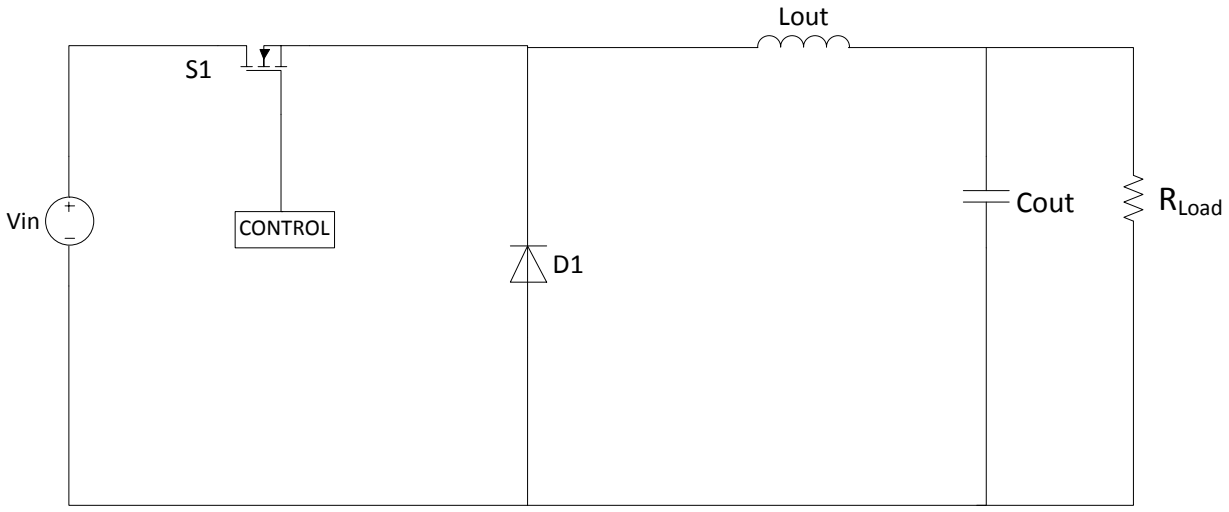


Figure 27: Basic Buck Converter

The SSSR is used to replace the free-wheeling diode D1 in the buck converter so that its effectiveness can be tested. The circuit diagram of the SSSR implemented on the conventional buck converter is shown below in Figure 28.

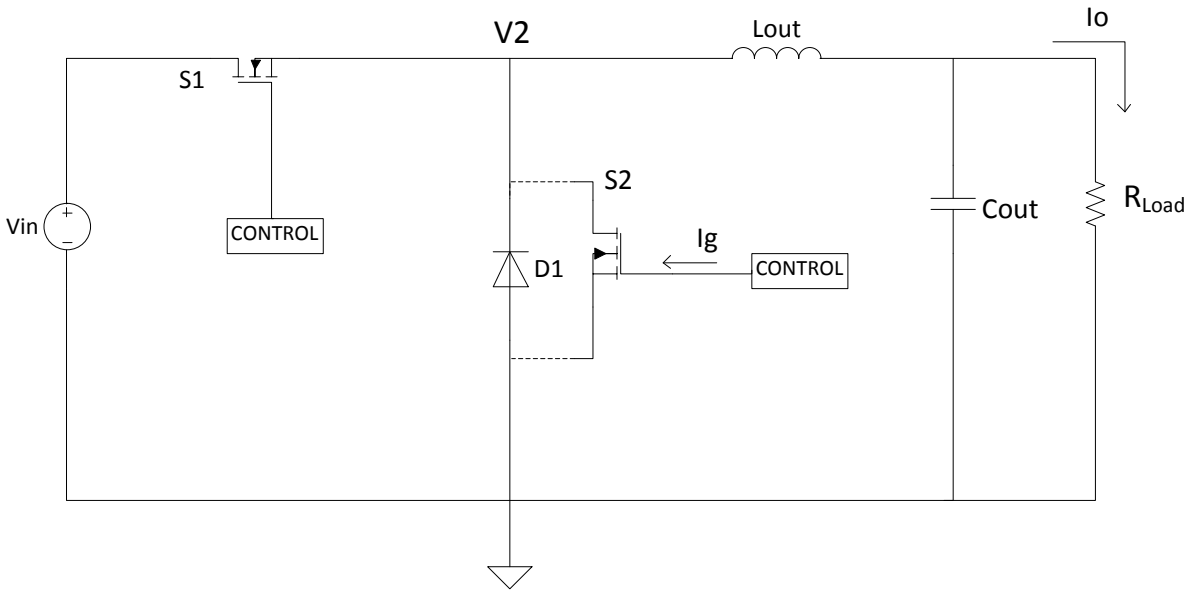


Figure 28: SSSR Implemented on the Conventional Buck Converter.

5.4 Summary

This chapter starts with identifying the problem in the power supply and by defining the problem statement in depth. It then proposes and introduces a new device called the Self Sustained Synchronous Rectifier (SSSR) to cost-effectively address all the concerns that have been defined and laid out by the problem statement. The operation and working of the SSSR has been explained in detail. Then the circuit diagram to be used to realize the SSSR discretely has been proposed and the various components and their workings explained. Finally, a test bed has been proposed to implement the SSSR and test its effectiveness. The next chapter presents the simulation and experimental results for the SSSR.

CHAPTER 6

SIMULATION AND EXPERIMENTAL RESULTS

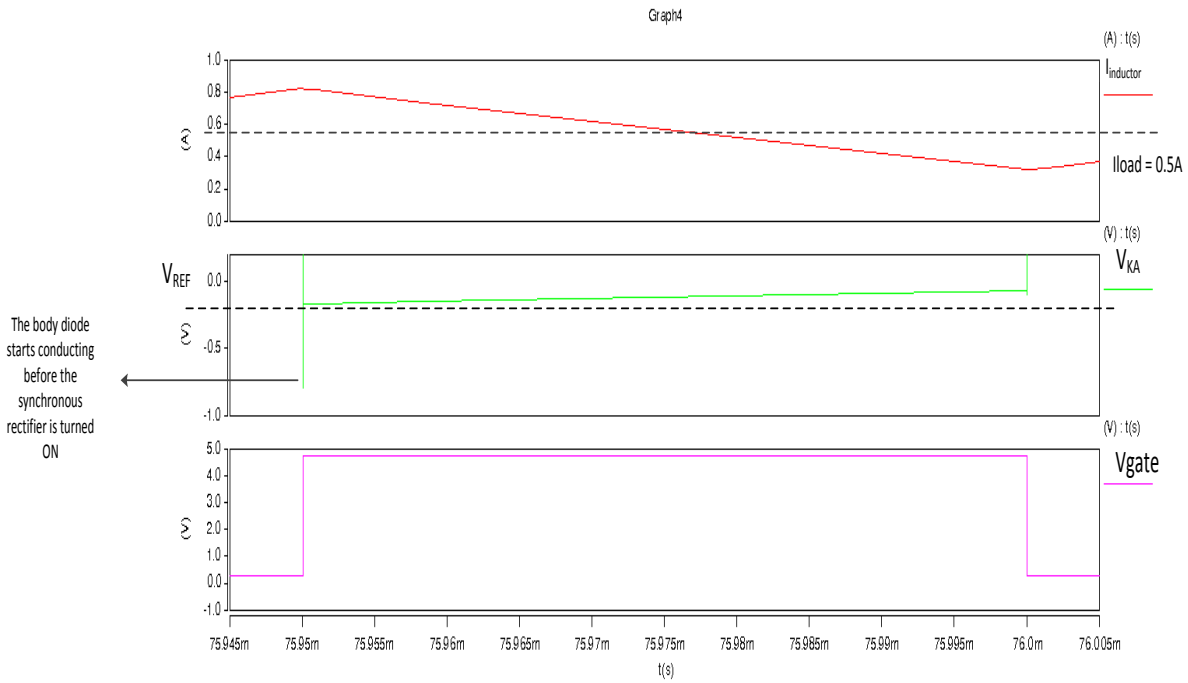
6.1 Simulation Results

The SSSR and the corresponding test bed circuitry were implemented and simulated using the SABER simulation package. The circuit parameters and operating conditions used in the simulation are summarized below in Table 14.

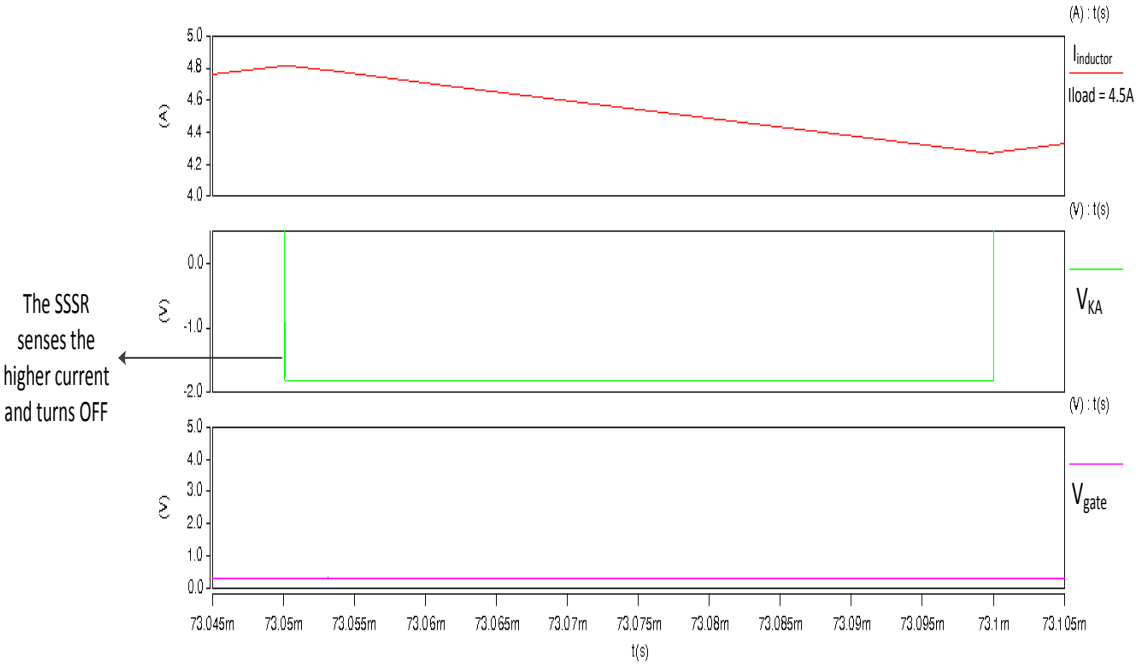
Table 14: Circuit Parameters and Operating Conditions used in the Simulation Circuit

S. No	Circuit Parameter	Value
1	Input Voltage (Vin)	10V
2	Unregulated Output Voltage (Vout)	5V
3	Switching frequency	10kHz
4	V_f of freewheeling diode D1	1.8V
5	$R_{DS\ (ON)}$ of Synchronous MOSFET used in SSSR	200mΩ
6	Reference current (I_{REF})	1A

The simulation results obtained are shown below in Figures 29 (a) and (b).When the primary switch is turned OFF, initially the body diode starts to conduct as shown in Figure 29 (a). However this is sensed by the SSSR which immediately turns ON the synchronous rectifier switch of the SSSR. Now, the body diode's voltage gets clamped by the conduction voltage of the synchronous switch which is less than the ON state forward voltage drop of the diode (V_f) and hence the diode remains turned OFF.



(a)



(b)

Figure 29: Waveforms of the SSSR when (a) Load Current is less than the Reference Current (b) Load Current is greater than the Reference Current

Also, as the load current is less than the reference current in this case, the synchronous switch remains ON for that entire switching cycle. However if the load current is greater than the reference current, the current sense circuit senses this and turns OFF the synchronous MOSFET as shown in Figure 29 (b).

The simulation results demonstrate that the circuit and principle of the SSSR are working.

6.2 Laboratory Testing and Experimental Results

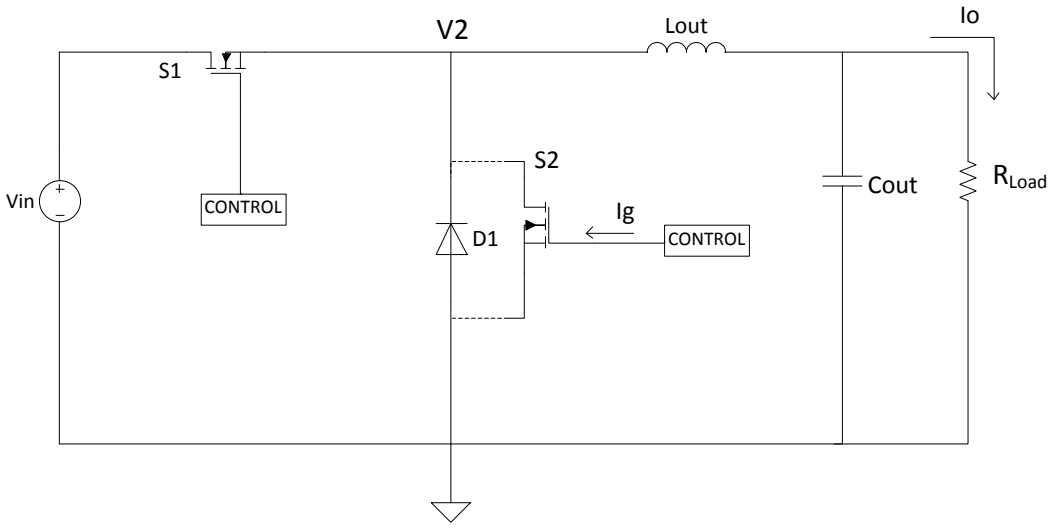
The test bed was built inside the lab using a prototyping board and the SSSR was implemented using discrete components. The results below validate the effectiveness of the SSSR in the laboratory.

The circuit parameters and the operating conditions of the SSSR and the test bed used in the laboratory are detailed below in Table 15.

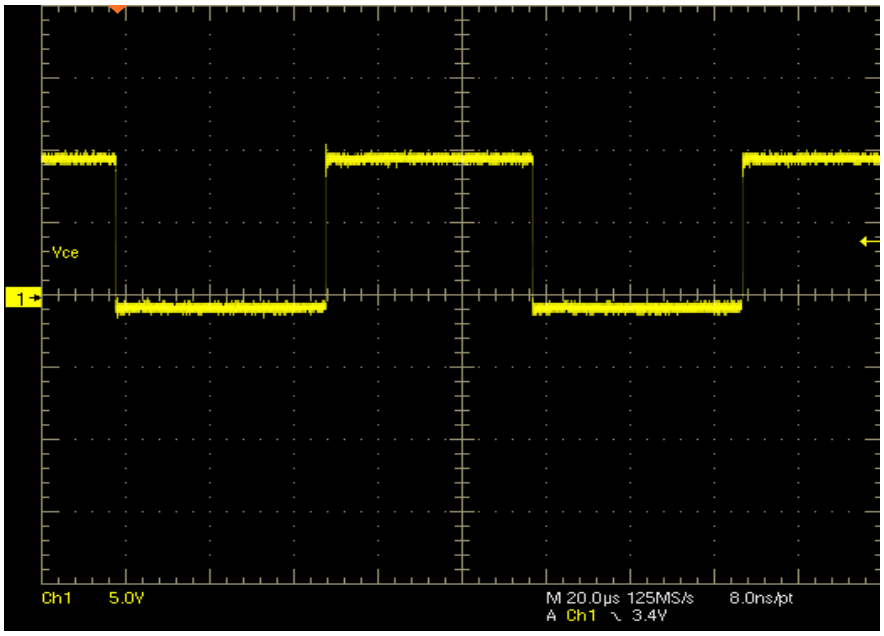
Table 15: Circuit Parameters and Operating Conditions of the Experimental Test Setup

S. No	Circuit Parameter	Value
1	Input Voltage (Vin)	10V
2	Unregulated Output Voltage (Vout)	5V
3	Switching frequency	10kHz
4	V_f of freewheeling diode D1	0.6V
5	$R_{DS\ (ON)}$ of Synchronous MOSFET used in SSSR	50mΩ
6	Reference current (I_{REF})	2A
7	Duty Cycle of Conduction	0.5

In Figure 30, the circuit diagram of the buck converter (without the SSSR) with the voltage across the diode rectifier is shown.



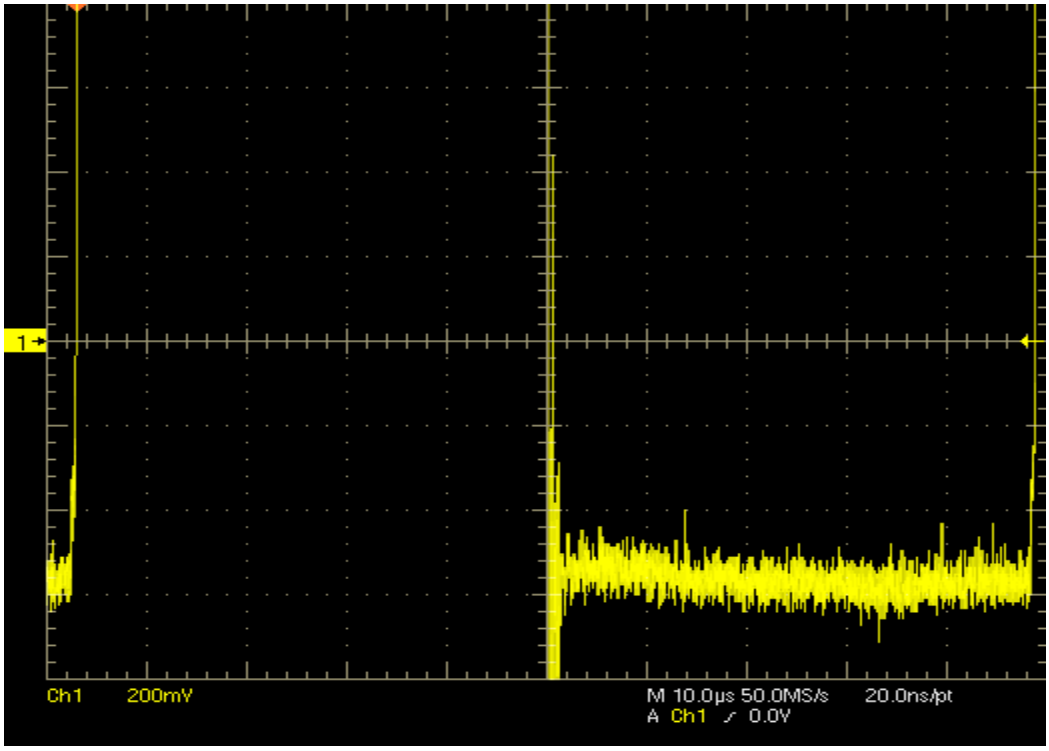
(a)



(b)

Figure 30: (a) Test Bed- Basic Buck Converter (b) Voltage V2 across the Diode Rectifier.

(c) Voltage V2 across the Diode Rectifier when the Diode is Conducting



(c)

Figure 30 continued: (a) Test Bed- Basic Buck Converter (b) Voltage V2 across the Diode Rectifier (c) Voltage V2 across the Diode Rectifier when the Diode is Conducting

The Figure 30 (c) above shows the voltage V2 across the diode, in a buck converter without the SSSR. There is a voltage drop of nearly -0.6V, when the diode is conducting.

The SSSR is now implemented on the test bed by paralleling it across the terminals of diode D1. During light load conditions, when the load current Io is less than the reference current I_{REF}, the switch S2 (of the SSSR) conducts and hence almost completely eliminates the loss due to the diode rectifier. This is shown in Figure 31 where under light loading conditions (I_{LOAD} (=1A) < I_{REF} (=2A)) switch S2 conducts and hence the voltage across the diode rectifier is $V_{KA} \approx 0$.

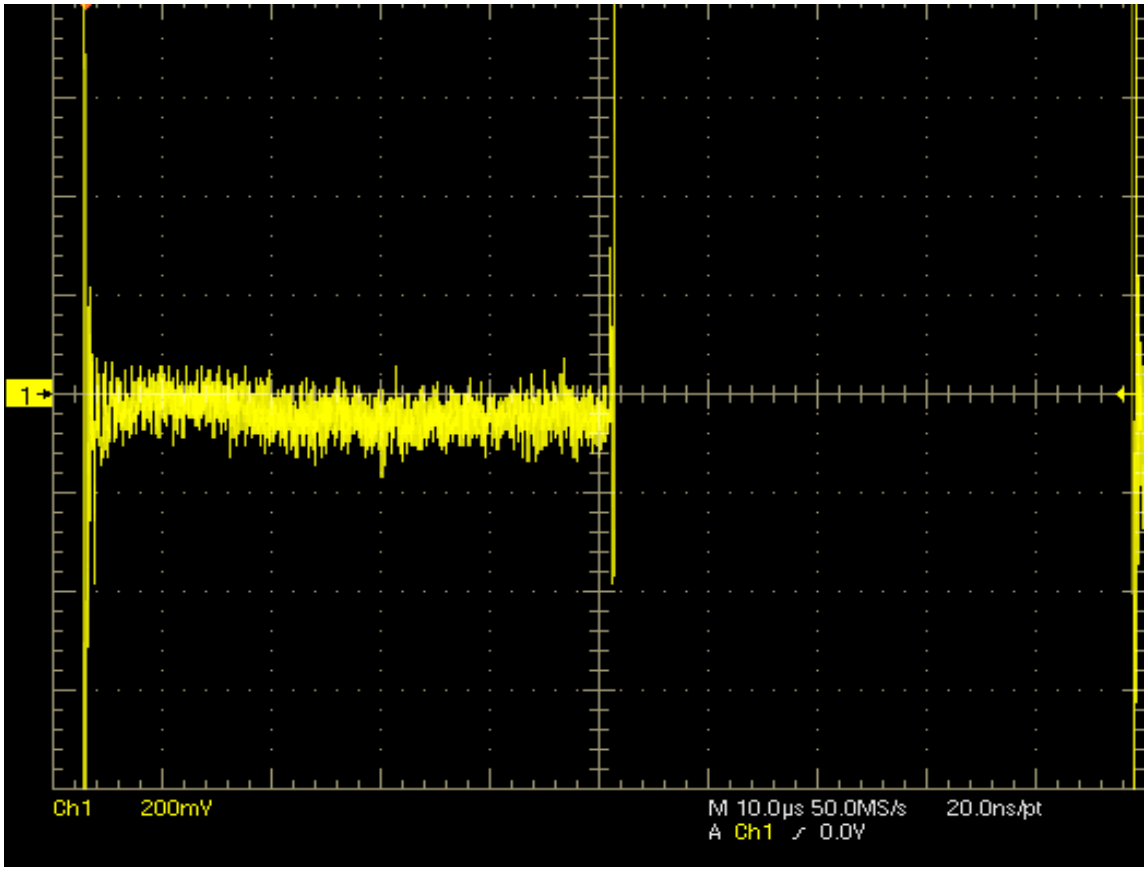


Figure 31: Voltage across the SSSR under Light Load Conditions.

However when the load current becomes greater than the reference current, the switch S2 turns OFF and allows the diode to conduct. This feature of the SSSR is illustrated in Figure 32 where the load current (=2.5A) is greater than the reference current (=2A) and hence the switch S2 turns OFF and the diode conducts resulting in a voltage drop of $V_{KA} \approx -0.6V$ across the SSSR.

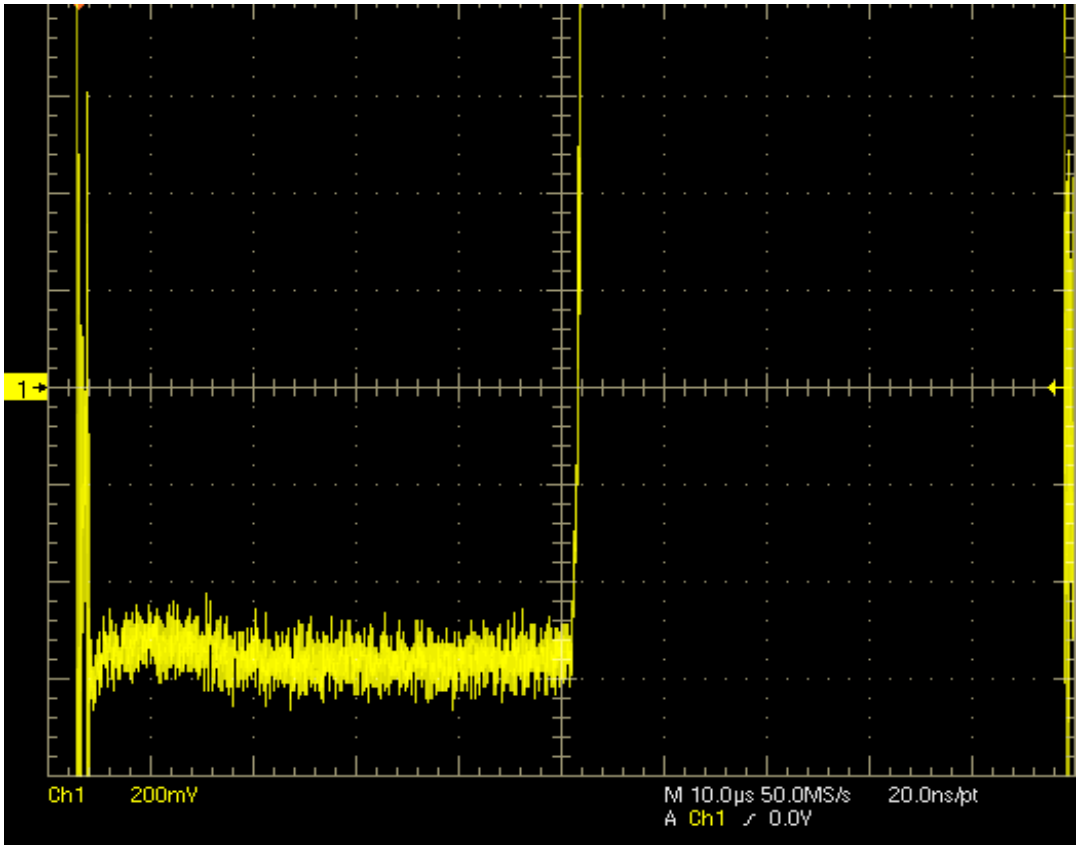
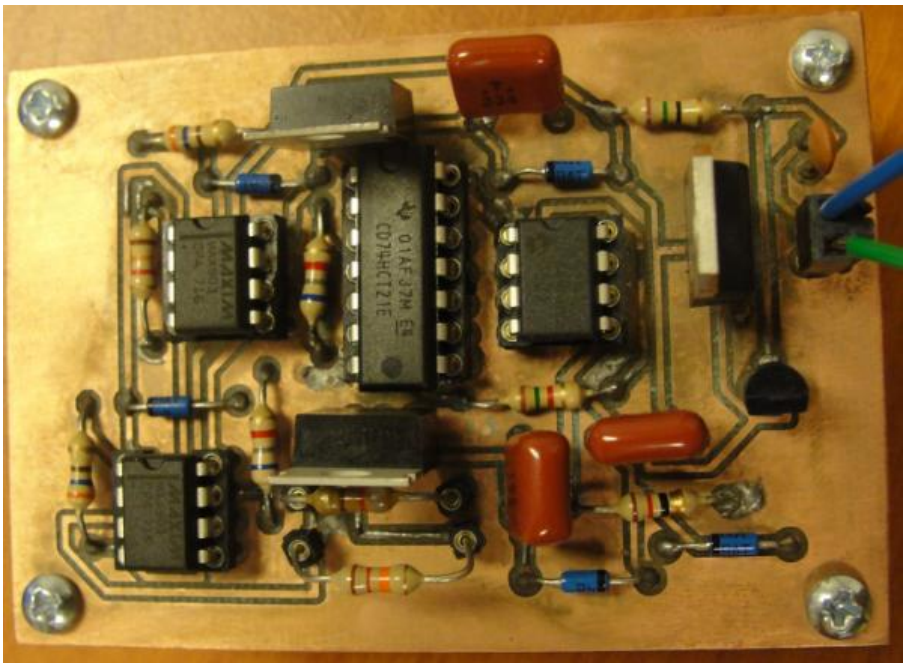


Figure 32: Voltage across the SSSR under Heavy Loading Conditions.

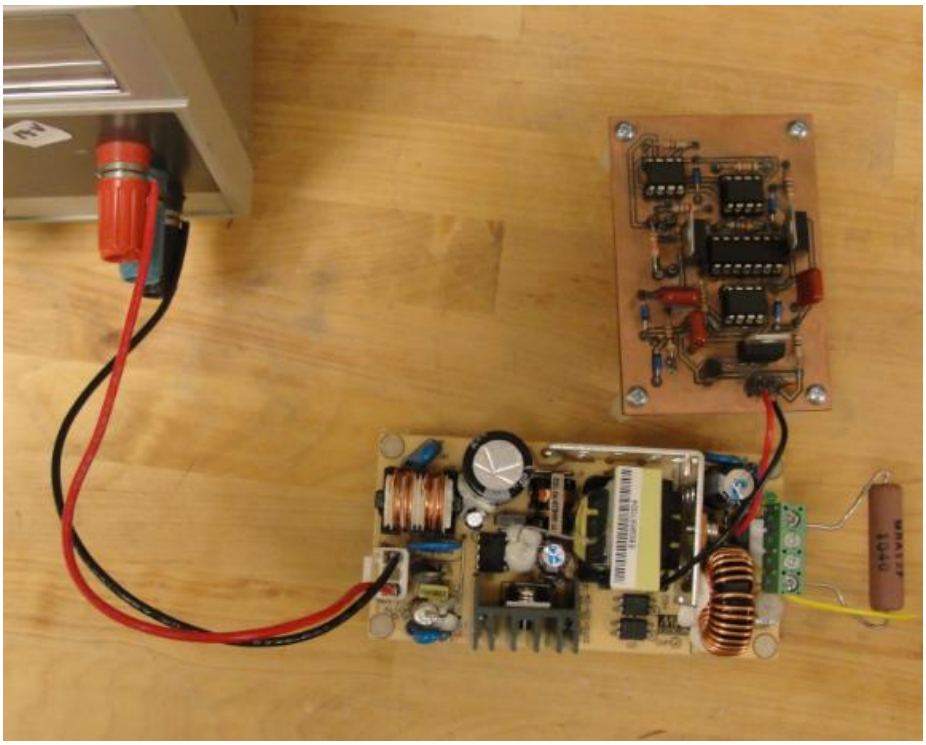
The results obtained from Figures 31 and 32 clearly demonstrate the working of the SSSR on the laboratory test bed.

6.2.1 Testing of SSSR on a Commercial Power Supply.

Since the working of the SSSR has been demonstrated on a laboratory test setup, the prototype of the SSSR is now tested on a commercially available dc-dc converter. The photographs of the SSSR proof of concept board and that of SSSR being tested on a commercial power supply are shown in Figures 33 (a) and (b).



(a)



(b)

Figure 33: (a) Proof of Concept Two Terminal SSSR Board (b) SSSR being Implemented and Tested on a Commercial Power Supply

The circuit parameters and operating conditions of the commercial power supply are shown below in Table 16.

Table 16: Circuit Parameters and Operating Conditions of the Commercial Power Supply

S. No	Circuit Parameter	Value
1	Input Voltage (Vin)	10V
2	Regulated Output Voltage (Vout)	5V
3	Switching frequency	83kHz
4	V_f of freewheeling diode D1	0.45V
5	$R_{DS\ (ON)}$ of Synchronous MOSFET used in SSSR	50mΩ
6	Reference current (I_{REF})	2A

The operation of the commercial dc-dc power supply with and without the SSSR are illustrated in Figures 34 and 35.

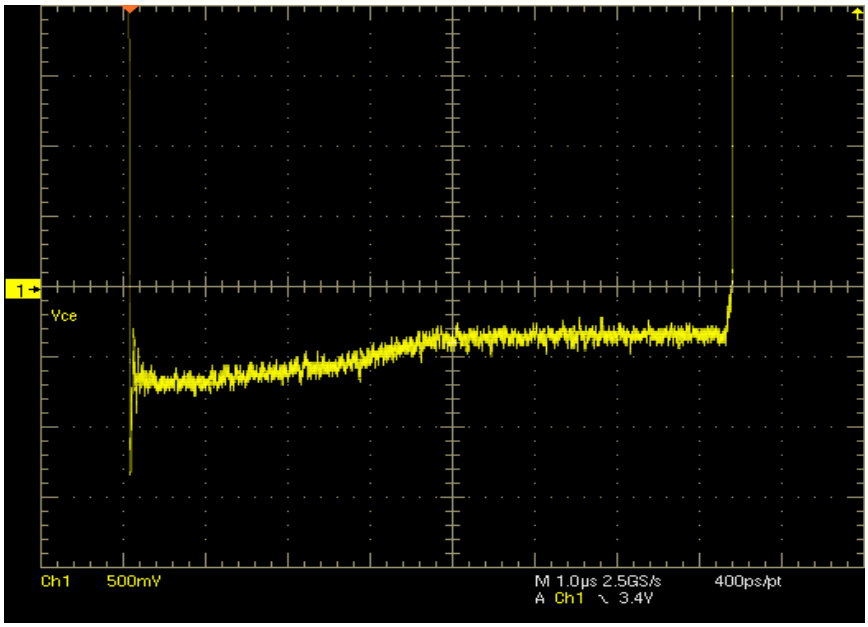
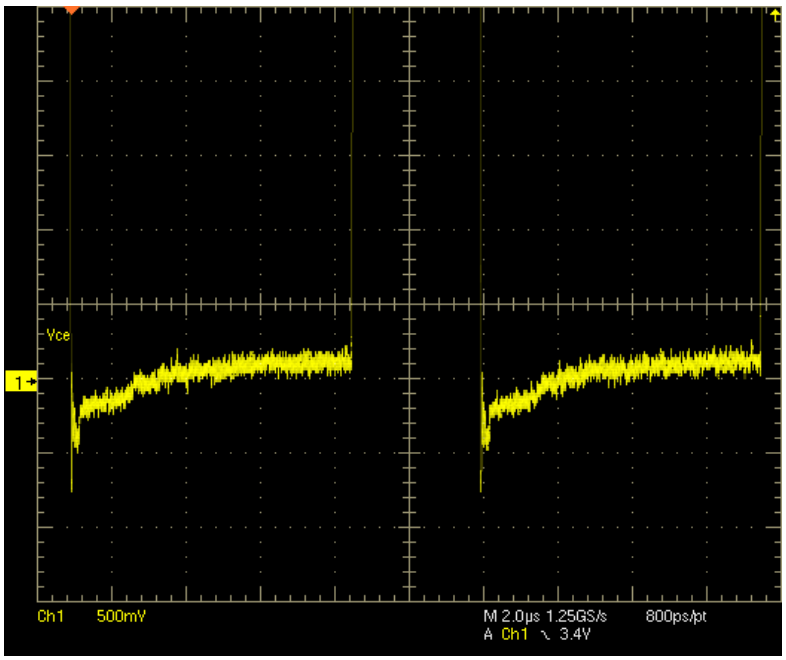
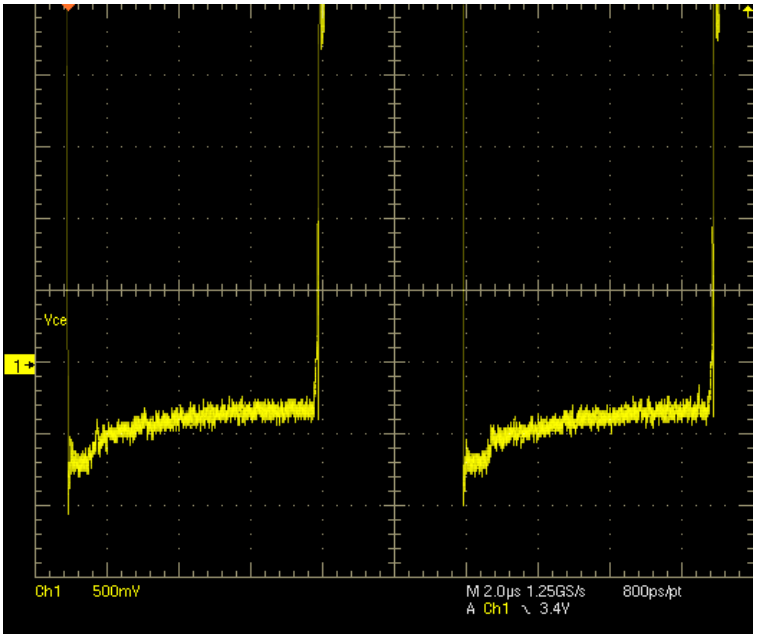


Figure 34: Voltage across Diode Rectifier in the Commercial Supply without the SSSR



(a)



(b)

Figure 35: Voltage across Diode Rectifier in a Commercial Power Supply Augmented with the SSSR under (a) Light Load (I_{LOAD} = 1A) (b) Heavy Load Conditions (I_{LOAD} = 5A)

From Figures 34 and 35 it can be clearly seen that the SSSR works as proposed in eliminating the voltage drop across the diode rectifier terminals of the commercial dc-dc Converter under light load conditions. The working of the SSSR has been demonstrated in the laboratory as well as on a commercial product over a frequency range of 10 – 83 kHz.

6.3 Comparison of Losses in a system with and without SSSR.

The benefits of augmenting the output diode rectifier with the SSSR are determined by computing and comparing the losses across the diode rectifier with and without the SSSR. The losses are computed and compared for the buck converter test bed. The condition under which the test bed is operated is shown in Table 15. The system is operated under light load conditions (Load current = 2A).

6.3.1 Operation without SSSR

When the system is operated with the diode rectifier, the energy lost in the diode rectifier is in the form of conduction losses. The conduction loss across the diode is given by the formulae $V_f \times I_d \times D$, where V_f is the forward voltage drop across the diode, I_d is the current through the diode (in this case I_d = load current) and D is the duty cycle of conduction. The forward voltage drop across the diode as seen from Figure 6-5 is 0.6V. So, the conduction loss in the diode rectifier = $0.6 \times 2 \times 0.5 = 0.6$W.

6.3.2 Operation with SSSR

In this case the diode rectifier of the test bed is augmented with the SSSR. The synchronous switch of the SSSR conducts, since the load current (= 2A) is less than or

equal to the reference current (=2A) and thus prevents the diode across it from conducting.

The energy that is lost in the SSSR can be classified into (a) Conduction losses and (b) Power that is required to control and drive the SSSR.

6.3.2.1 Conduction Losses

The conduction losses in the SSSR is due to the conduction of the synchronous switch and is given by the formulae $I_{SW}^2 \times R_{DS\ (ON)} \times D$, where I_{SW} is the current through the synchronous switch (in this case, $I_{SW} = I_{LOAD}$) and $R_{DS\ (ON)}$ is the ON-state resistance of the MOSFET. So the conduction loss in the SSSR, $P_{cond} = 2^2 \times 0.05 \times 0.5 = 100mW$.

6.3.2.2 Control and Drive Power Losses

Power is required to control and drive the synchronous MOSFET that is used in the SSSR. The SSSR has been carefully designed so as to minimize the amount of effort and power that is required to control and drive itself. The control and drive circuits are powered by both a positive (V_{CC}) and a negative (V_{ee}) voltage rail. The power consumed by both these supply rails is computed separately. To measure the power lost in the positive rail, a small resistance R2 (=2.2Ω) is added to the positive rail's charging circuit as shown in Figure 36.

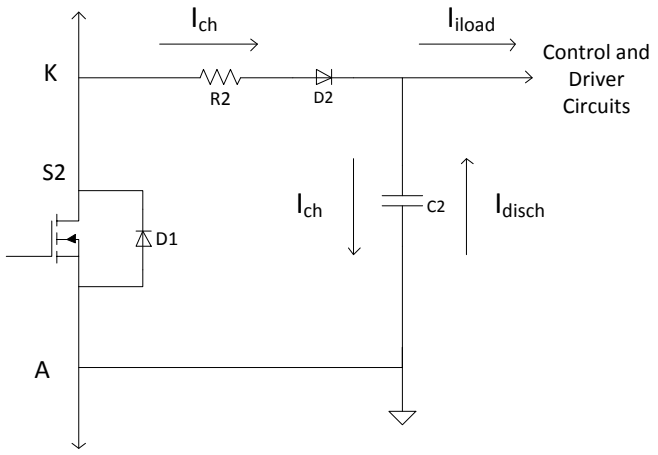


Figure 36: Measurement of Power Lost in the Circuits Supplied by V_{CC}

The Capacitor C2 in the circuit above acts as the energy storage capacitor, storing energy from the external circuit and delivering that energy to the load. This capacitor voltage is regulated and used to supply the control and drive power loads that require a positive V_{CC} supply. The load in this circuit represents the power that is consumed by the internal control and drive loads connected to the positive supply rail. The power consumed by this load (P_{CD}) is computed by calculating the energy delivered to the capacitor (ΔE) during each switching cycle. This can be computed by using the formulae $P_{CD} = \Delta E = I_{ch} \times V_{C2}$, where I_{ch} is the charging current of capacitor C2 and V_{C2} is the voltage across capacitor C2. The charging current I_{ch} is obtained by measuring the voltage across the resistance R2 as $I_{ch} = V_{R2} / R2$. For the given test bed and operating conditions, the measured voltage across the resistance R2 for one switching cycle has been shown in Figure 37.

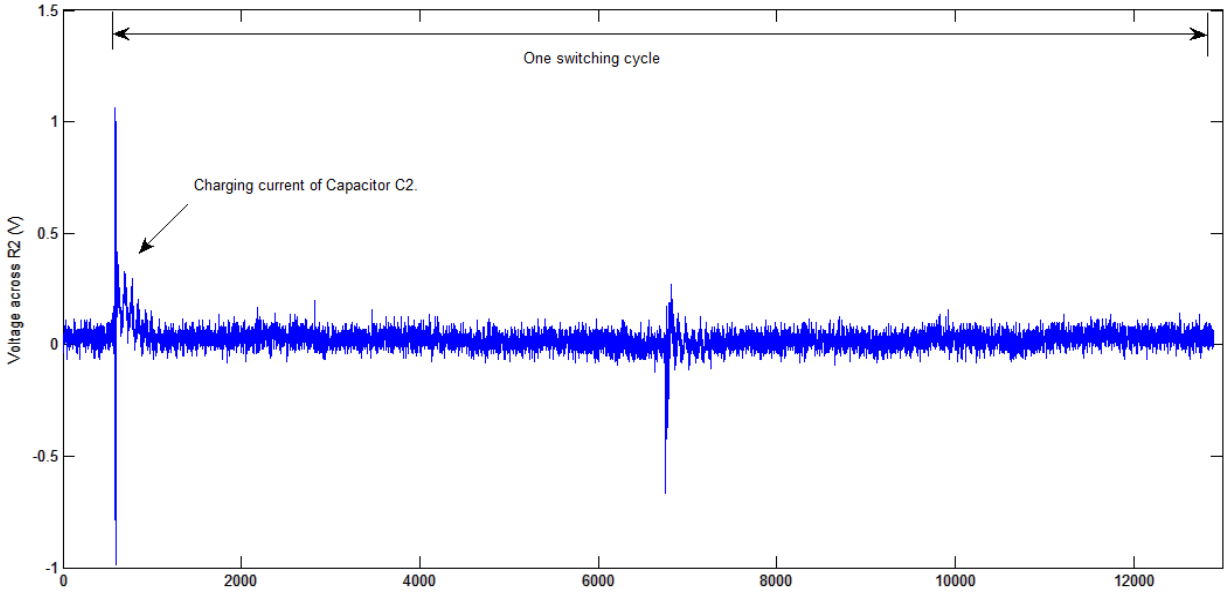


Figure 37: Voltage V_{R2} for One Switching Cycle.

The average value of V_{R2} is computed to be 7.55mV. The charging current I_{ch} is computed as $I_{ch} = 7.55/2.2 \times 10^{-3} = 3.43$mA and the average voltage across the capacitor C2 is measured to be 9.19V. So the power lost in this internal load P_{CD} is found to be equal to $\Delta E = I_{ch} \times V_{C2} = 3.43 \times 10^{-3} \times 9.19 = 31.5$mW.

Similarly, the power lost in supplying the control and drive power loads connected to the negative voltage rail V_{ee} can be computed. The average value of V_{R2} and the charging current are computed to be 3mV and 1.36mA ($I_{ch} = 3/2.2 \times 10^{-3)}$.The average voltage across the capacitor C2 is measured to be 7.54V. So the power lost in this internal load P_{ED} is found to be equal to the energy supplied to the capacitor in one switching cycle, $\Delta E = 1.36 \times 10^{-3} \times 7.54 = 10.28$mW. The total power dissipated in the SSSR under the specified operating conditions is found to be

$$P_{SSSR} = P_{cond} + P_{CD} + P_{ED} = 100 + 31.5 + 10.28 = 141.7\text{mW}.$$

6.3.3 Comparison of Losses

Under the specified operating conditions, the total power lost in the diode rectifier is observed to be 600mW whereas the total power lost in the SSSR is 142mW. From the results obtained it can be seen that the use of SSSR reduced the energy lost in the diode rectifiers by 75%. A savings of 450mW has been achieved for this system under loading conditions and a reference current of 2A. The design of the SSSR can be modified to accommodate higher reference currents depending upon the type of application it is to be used for and after performing a cost benefit analysis to determine whether the energy saving obtained offsets the costs involved in upgrading to a higher current synchronous switch in the SSSR.

6.4 ROI Analysis

A preliminary return of investment analysis has been done taking into consideration that 450mW of continuous power usage is saved by using a SSSR in this test bed under the light load condition. Then the amount of savings in energy for the test bed system obtained by using the SSSR over a period of one year = energy saved per hour × number of hours in a year = 450mWhr × 24 × 365 = 3.94kWhr. The cost of power in the state of Georgia is approximately 10 cents per kWhr. Then the cost at which the SSSR has to be priced to break even within periods of 1 to 5 years is shown in Figure 38.

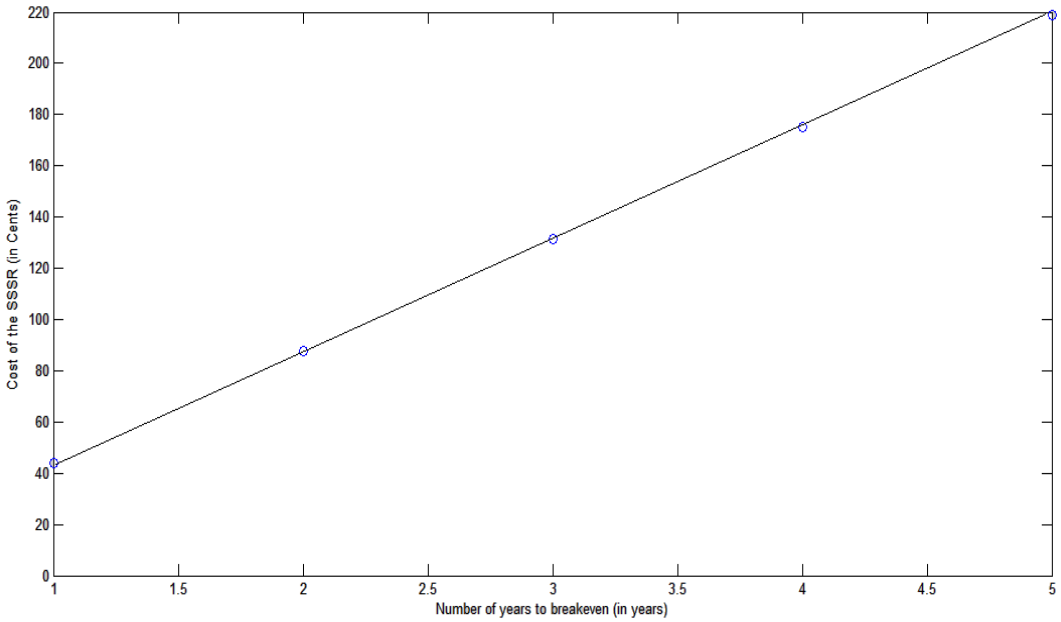


Figure 38: Number of Years to Breakeven with the Cost of the SSSR.

The system wide impact of using the SSSR is tremendous. For e.g. If the power supply of every new printer sold in the U.S is augmented with this two terminal device, and if the conservative estimate of 450mW of continuous power savings obtained for the test bed is extended for the printers, then the amount of energy saved per year in the printers in the U.S alone is a staggering 104GWhr. That is the equivalent of preventing a hundred thousand tons of CO_2 from reaching the atmosphere [33].

6.5 Summary

In the first part of the chapter, the circuit of the SSSR was simulated using the SABER package to validate its operating principles. Next, the SSSR was built using discrete components and tested on a test bed built in the lab. Once the proof of concept device was proven to be working, a board version of the SSSR was made and implemented on a commercial dc-dc power supply and its effectiveness proven. The

benefits of augmenting a diode rectifier with the SSSR were further demonstrated by analyzing the percentage savings in energy obtained by the use of SSSR. Finally a preliminary ROI analysis was created for the SSSR and the impact of its use shown on a system wide scale.

CHAPTER 7

CONCLUSION AND FUTURE WORK

The main focus of this research work was to show that redesigning of the existing power supplies towards a more energy efficient design is both technically feasible and economically viable. As an initial part of this work, computer and printer power supplies were identified as the main target applications. Several high level and low level tests were conducted on multiple commercially available units across various price ranges. It was seen that even under the most conservative assumptions and estimates 3.68TWhr of energy is consumed by commercial grade multi functional printers while the energy consumed by household printers is around 1.96TWhr in the idle mode of operation in the US alone every year. In the personal computing arena, the amount of energy wasted in the home and office computers are seen to be 34GWhr and 350GWhrs respectively. The important factor in the above projections are that this energy is being consumed or wasted when these appliances are not in active use but under idle mode of operation. Definitely a market exists for redesign of the power supplies since more than 1TWhr of energy is being wasted in the power supplies of electronic appliances in the US when they are not doing any amount of useful work**.**

A new device called self sustained synchronous rectifier (SSSR) has been devised. It is a two terminal device that has been proposed to cost effectively improve the efficiency of the power supplies. The proposed device is cheap, self-controlled, self-powered, and has high impact in mitigating the losses in the power supply. The device consumes minimal space and can be easily augmented to any external power supply regardless of the type of the converter used. A proof of concept board of the device is

built using discrete components and its effectiveness proven on a commercial dc-dc power supply. Even under the most conservative estimates the cost of the SSSR is offset by the direct savings in energy. However, the impact when this device is implemented on a system wide scale is found to be tremendous. The implementation of just this one device in all the new printers being shipped in the US alone will save 104GWhr of energy in one year from being wasted in power supplies. That is equivalent of relieving the atmosphere from a hundred thousand tons of CO_2 burden. If the device is adopted on a nationwide scale it could have a wide impact in reducing the carbon foot print of the electronic devices on the U.S power grid and that of the power grid on the atmosphere.

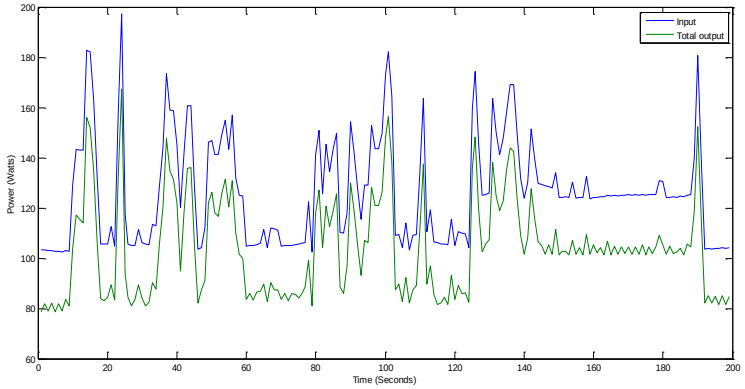
As part of the future work, the discretely built device can be accommodated into a single IC so as to make the SSSR commercially viable. A detailed cost benefit analysis can be done after taking the costs involved in producing the SSSR into consideration.

APPENDIX A

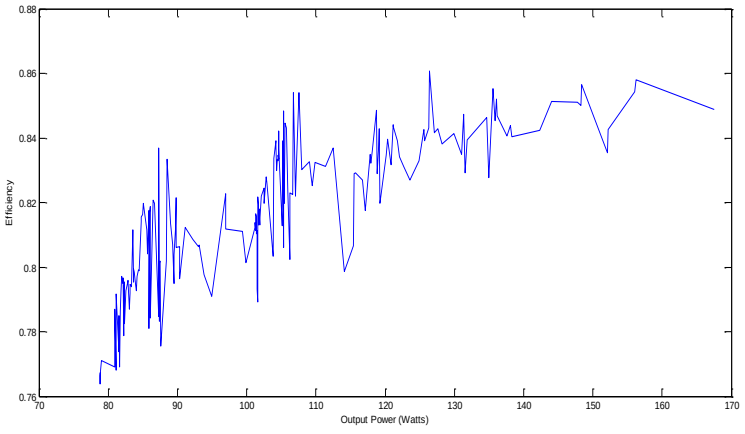
COMPUTATION OF ENERGY USAGE PROJECTIONS FOR HOUSEHOLDS

The input and output characteristics for three varied power supplies are shown below. They are obtained from measurements performed as detailed in Section 3.1.

Power Supply 1: Diablotek DA 350W Power Supply (Cost: $20)



(a)

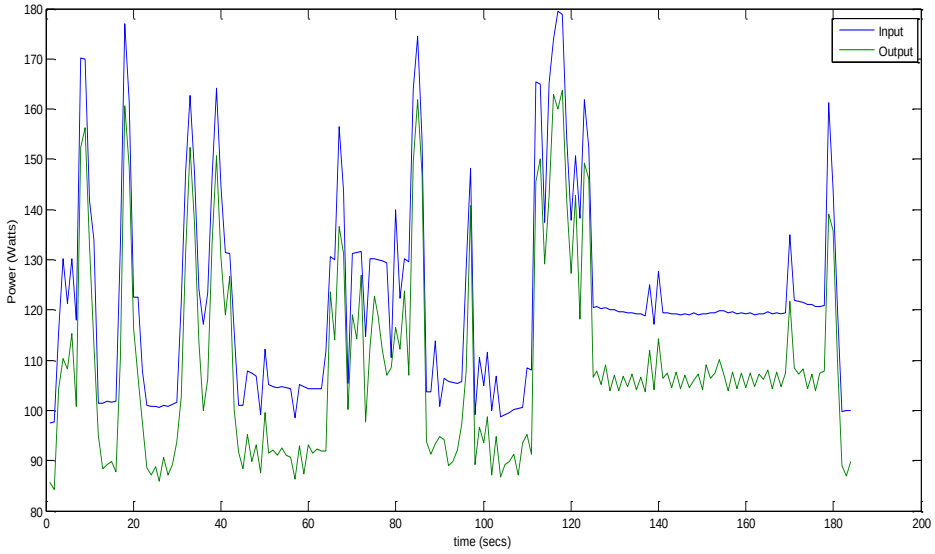


(b)

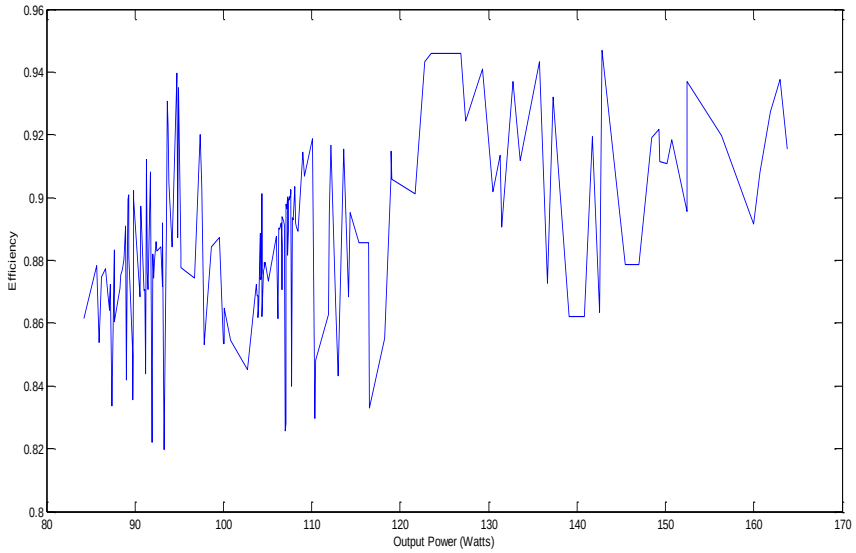
Figure 39: Characteristics of the Diablotek Power Supply (a) Input and Output Power vs. Time Curve (b) Efficiency vs. Output Power Curve

Power Supply 2: Antec –Basiq– 350 W Power Supply (Cost: $30)

PC loading: Usage of Internet based Applications for three minutes. (24 – 47% of full load)



(a)

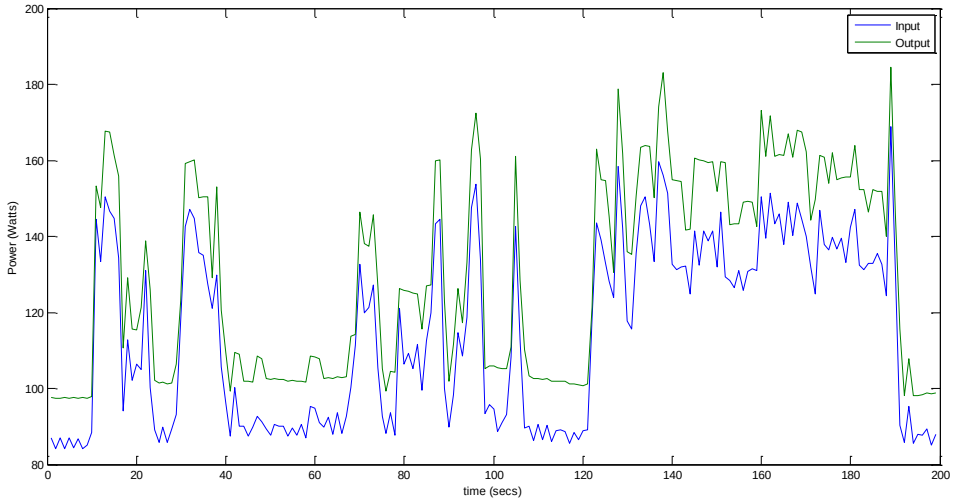


(b)

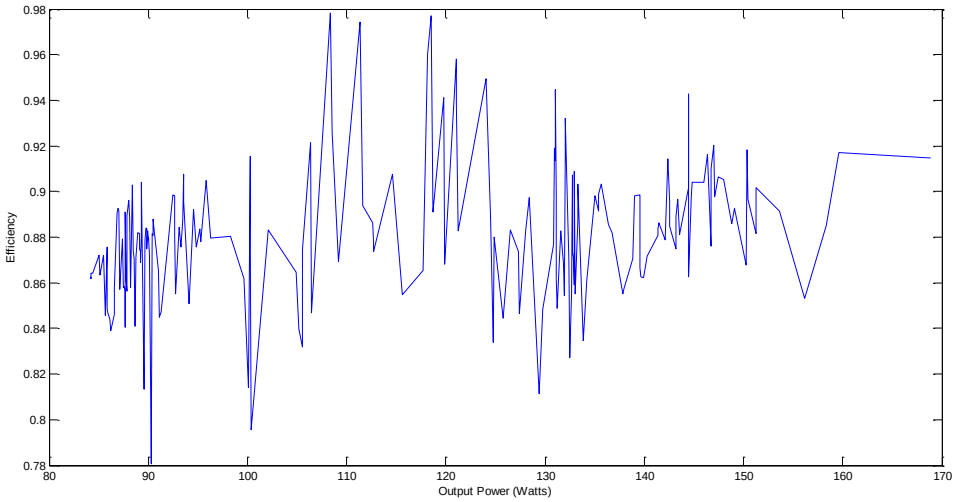
Figure 40: Characteristics of the Antec Power Supply (a) Input and Output Power vs. Time Curve (b) Efficiency vs. Output Power Curve

Power Supply 3: Thermaltake Lite Power Supply (Cost: $35)

PC loading: Usage of Internet based Applications for three minutes. (24 – 47% of full load)



(a)



(b)

Figure 41: Characteristics of the Thermaltake Lite Power Supply (a) Input and Output Power vs. Time Curve (b) Efficiency vs. Output Power Curve

The Figures above contain data representing the amount of energy consumed by each of the three power supplies while supplying a predefined load for three minutes. The energy consumption and usage data obtained from the Figures 39, 40 and 41 were used to compute the energy usage projections for households for a year.

The data from the paper [30] suggests that globally, in an average household the computer is used 23 days a month on average. During this time, it is powered on for 7 hours and 34 minutes of which it is used effectively only for 2 hours and 51 minutes. The data also suggests that 63% of time spent by the user is on internet usage. The energy usage projections have been computed by approximating (the other applications or loads also have an approximately similar profile as the internet usage profile) the entire effective usage time of the user to their internet usage. The computations for the energy usage and waste projections for three different power supplies have been shown below.

A.1 Power Supply 1 – Diablotek-350W

The energy usage and waste projections during the active mode operation of the power supply have been shown below. The computations were performed by using the data from Figure 39 (a)

Energy spent during three minutes of active usage = 8.34 Watt-hours.

Energy wasted during three minutes of active usage = 1.86 Watt-hours.

Approximate projection of energy spent per year = 5.7 kWh.

Approximate projection of energy wasted per year = 1.27 kWh

The energy usage and waste projections during the power supplies' idle mode operation have been detailed below.

Time spent idling in a year = (7h 34mins – 2h 51mins) × 12 = 56 hrs and 36mins.

Energy spent in idling time = 113.8 × 56.6 = 6.44 kWh.

Energy wasted during idling = (113.8 – 85.3) × 56.6 = 1.61 kWh

A.2 Power Supply 2 – Antec Basiq-350W

The energy usage and waste projections during the active mode operation of the power supply have been shown below. The computations were performed by using the data from Figure 40 (a)

Energy spent during three minutes of active usage = 7.74 Watt-hours.

Energy wasted during three minutes of active usage = 1.35 Watt-hours.

Approximate projection of energy spent per year = 5.29 kWh.

Approximate projection of energy wasted per year = 0.92 kWh

The energy usage and waste projections during the power supplies' idle mode of operation have been detailed below.

Time spent idling in a year = (7h 34mins – 2h 51mins) × 12 = 56 hrs and 36mins.

Energy spent in idling time = 107.1 × 56.6 = 6.06 kWh.

Energy wasted during idling = (107.1-85.77) × 56.6 = 1.21 kWh

A.3 Power Supply 3 – Thermaltake Lite Power

The energy usage and waste projections during the active mode operation of the power supply have been shown below. The computations were performed by using the data from Figure 41 (a)

Energy spent during three minutes of active usage = 7.18 Watt-hours.

Energy wasted during three minutes of active usage = 0.85 Watt-hours.

Approximate projection of energy spent per year = 4.91 kWh.

Approximate projection of energy wasted per year = 0.58 kWh

The energy usage and waste projections during the power supplies' idle mode of operation have been detailed below.

Time spent idling in a year = (7h 34mins – 2h 51mins) × 12 = 56 hrs and 36mins.

Energy spent in idling time = 97.6 × 56.6 = 5.524 kWh.

Energy wasted during idling = (97.6-84.19) × 56.6 = 0.76 kWh.

A.4 Summary

The detailed computations for the energy consumption and waste projections for a year for three varied power supplies under active and idle modes of operation have been shown here. The results obtained have been tabulated in the Table 17 below.

Table 17: Energy Waste Projections for Computer Power Supplies - Summary

	Diablotek-350W	Antec – Basiq 350W	Thermaltake Lite Power
Energy wasted idling (kWh/year)	1.61	1.21	0.76
Energy wasted in active mode(kWh/year)	1.27	0.92	0.58

APPENDIX B

COMPUTATION OF LOSSES IN THE POWER SUPPLY

The circuit schematic of the power stage of the Antec-350W Power supply has been simulated using MATLAB in open loop mode to find the components or parts of the circuit in which most of the energy gets wasted. The simulation results are then used for loss calculation. The operating point at which the simulation was performed has been shown below in Table 18. This operating point was measured while the power supply is serving a PC that is idling.

Table 18: Operating Point of the Power Supply under Idle Mode of Operation

S. No	Parameter	Value
1	Input to the Power Supply	106W
2	Output of Power Supply	85.91W
3	Duty Cycle of the Power Transistors	0.25
4	Actual loss in the Power Supply	20.1W
5	Current drawn by the 12V output	5.146A
6	Current drawn by the 5V output	4.2A
7	Current drawn by the 3.3V output	2.176A

The current drawn by the outputs given in Table 18 takes into consideration both the current drawn by the loads as well as that drawn by the output resistances.

The circuit schematic of the Antec-350 watt power supply is shown below in Figure 42.

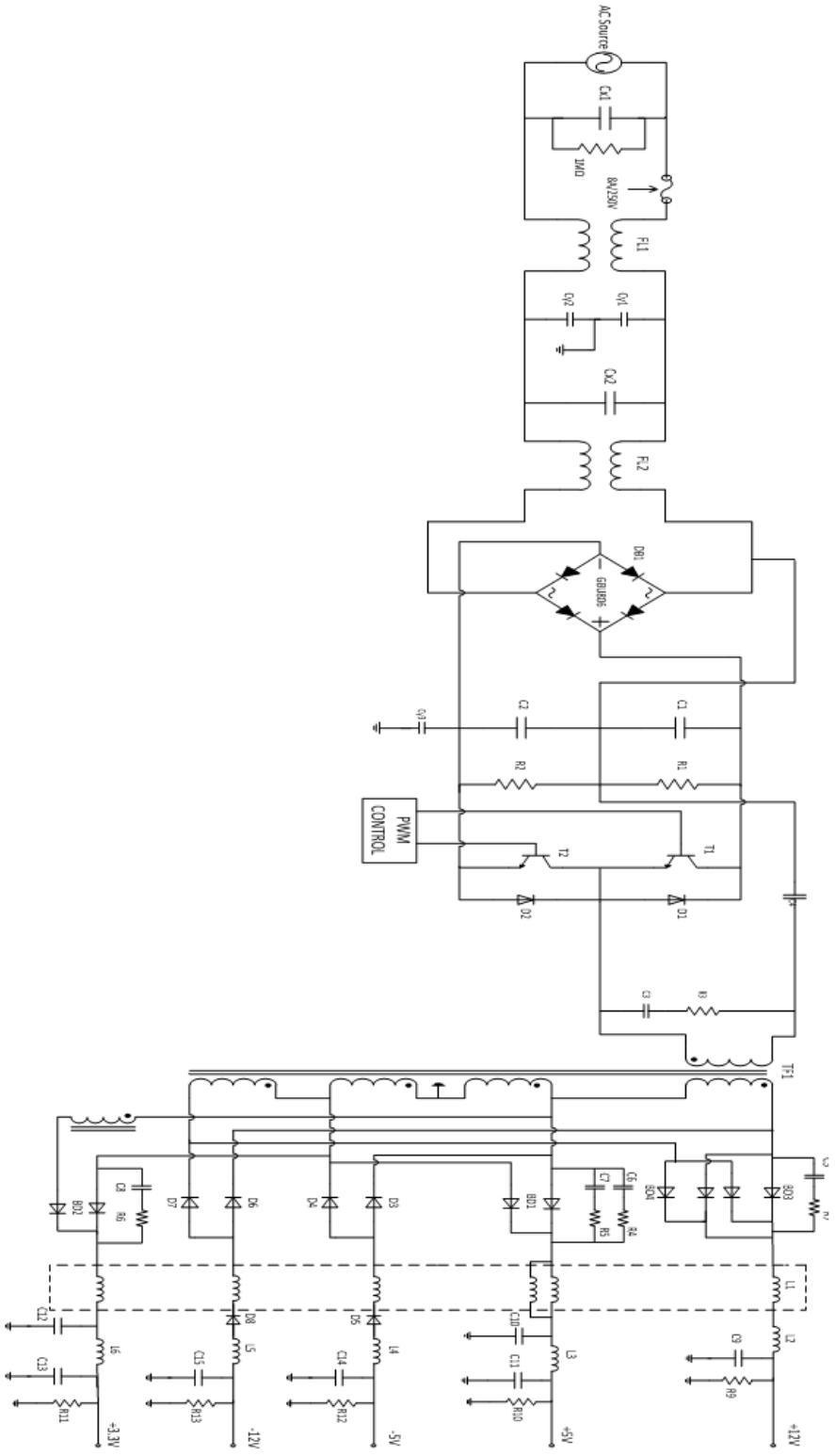


Figure 42: Schematic of the Power Stage of Antec–350W Computer Power Supply

The components used in the power stage of the circuit have been listed below in Table 19.

Table 19: Components used in the Power Stage of the Antec-350W Power Supply

S. No	Operation Stage	Component	Value/Part Number	Abbreviation
1	Transient Filtering Stage	Ferrite Coils		FL1,FL2
2		Fuse	8A/250V × (1)	F
3		Disc Capacitors	4.7nF × (2)	Cy1,Cy2
4		Metalized Polyester Capacitors	470nF × (2)	Cx1,Cx2
5	Voltage Doubler and Primary Rectifier.	Diode Bridge	GBU806 LT0205 × (1)	DB1
6		Disc Capacitor	4.7nF × (1)	Cy3
7		Electrolytic Capacitors	470uF × (2)	C1,C2
8		Resistors	62k × (2)	R1,R2
9	Switching Circuit	Power Transistors	D13009K × (2)	T1,T2
10		Resistor	51 ohms × (1)	R3
11		Disc Capacitor	2.2nF × (1)	C3
12		Disc Capacitor	1uF × (1)	C4
13		Transformer		Tf1
14		Diodes	PR1005 × (2)	D1,D2

15	Secondary Stage	Power Schottky Rectifier	STPS3045CT × (2)	BD1,BD2
16		Rectifier	HBR16200 × (2)	BD3,BD4
17		Diodes	FR1535 × (6)	D3-D8
18		Resistors	4.7ohms × (2), 5.6ohms × (1), 10ohms × (1)	R4,R5, R6,R7
19		Disc Capacitors	10nF × (4)	C5,C6,C7, C8
20		Inductors	400uH × (9), 1.2mH × (1)	L1-L9, L10
21		Electrolytic Capacitors	3.3mF × (1), 2.2mF × (4), 220uF × (2)	C9, C10-C13, C14,C15
22		Output Resistors	100ohms × (1), 15ohms × (1), 10ohms × (1) 10k × (2)	R8 R9 R10 R11,R12

B.1 Loss Calculation

The detailed calculation of the losses in the various components of the power supply under test has been shown below.

B.1.1 Output Resistors

The output resistors at the three main output voltage rails of 12V, 5V and 3.3V contribute most significantly to the losses amongst the resistors.

Power loss in the resistor R8 (100ohms) at 12V output $= \frac{12^2}{100} = 1.44W$

Power loss in the resistor R9 (15ohms) at 5V output $= \frac{5^2}{15} = 1.667W$

Power loss in the resistor R10 (10ohms) at 3.3V output $= \frac{3.3^2}{10} = 1.089W$

The total power lost in the output resistance is approximately 4.2W.

B.1.2 Cooling Fan

The cooling fan draws 0.18A current at 12V. So the power loss in the fan is equal to 2.16W.

B.1.3 Output Diode Rectifiers

The conduction losses in the diode rectifiers is calculated as $V_f \times I_d$, where V_f is the forward voltage drop across the diode and I_d is the current through the diode. The current through the rectifier diodes of the 12V output has been shown below. The yellow curve represents current through diode 1 of the rectifier while the pink one represents the current through diode 2. The white line represents the output current Io whereas the green line represents the current Io/2 when the output current splits equally between the two diodes. Hence it can be clearly seen from the graph that the average current through the rectifier for one switching cycle is equal to Io.

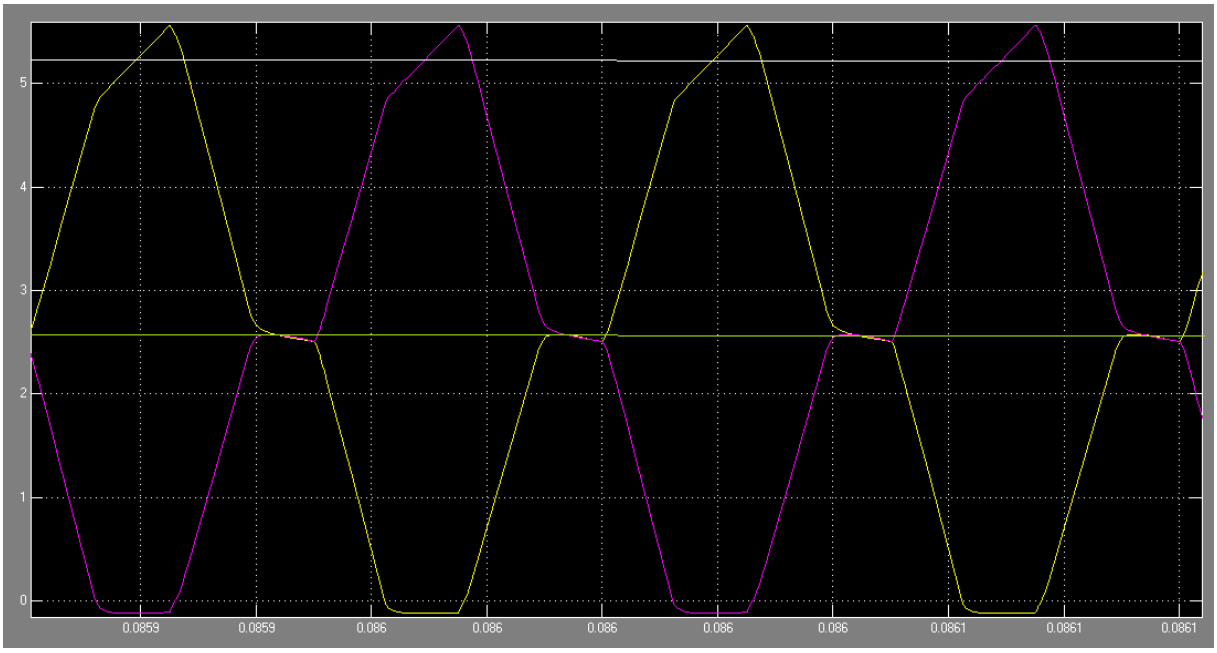


Figure 43: Current Waveforms of the Output Rectifier used in the 12V Output Stage

The net current through the rectifier is equal to the output current. The 12V output stage uses two HBR16200 rectifiers in parallel to support high currents. The forward voltage drop of this device as obtained from its datasheet is 1V. The 5V and 3.3V output stages each use 1 STPS3045CT rectifier which has a forward voltage drop of 0.57V.
The conduction loss in the rectifier of the 12V output stage = 1V × 5.146A = 5.146W.
The conduction loss in the rectifier of the 5V output stage = 0.57V × 4.2A = 2.4W.
The conduction loss in the rectifier of the 3.3V output stage = 0.57V × 2.176A = 1.24W.

The conduction loss of the rectifier used in -12V output stage has been neglected since the current drawn by this output is negligibly small. Hence the total power loss in the output rectifiers of the secondary stage is 8.79W.

B.1.4 Input Power Switches

Power transistors are used in the main switching circuit of this power supply. The power is lost in these transistor switches in the form of both conduction and switching losses.

B.1.4.1 Conduction Losses

The conduction loss in these transistors is calculated from the formulae $P_{cond} = V_{ce} \times I_c$, where V_{ce} is the voltage across the device and I_c is the current through the transistor. The current through these transistors has been shown below in Figure 44.

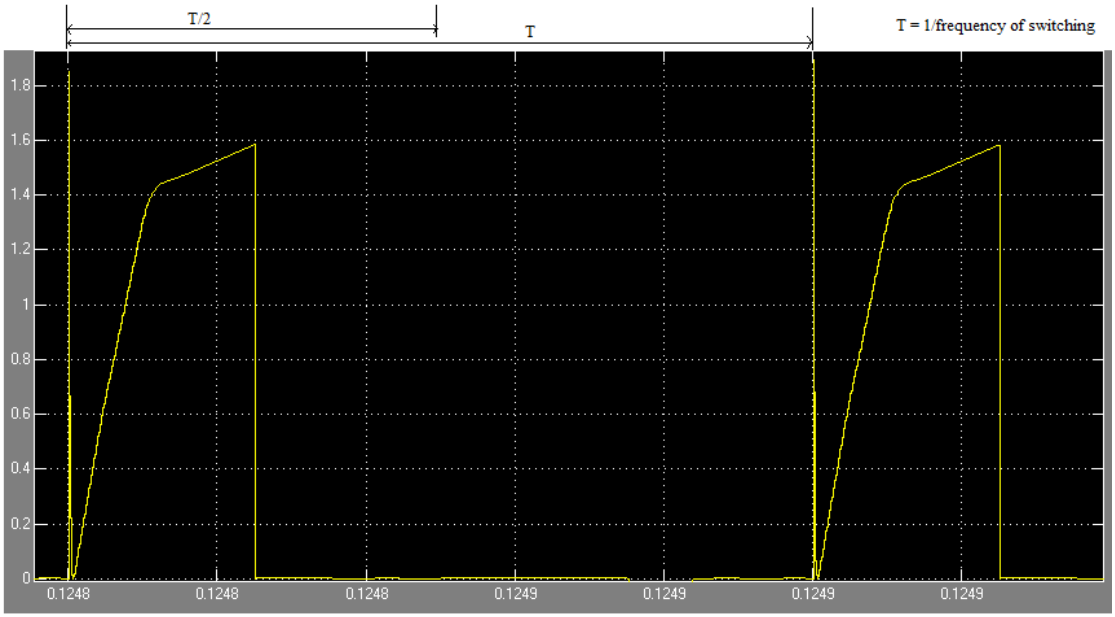


Figure 44: Current through the Upper Transistor Q1

The primary switching circuit employs two D13009K Power transistors. The current through the other transistor Q2 is the same as that of Q1 but is phase shifted by one half the time period of switching. The average current through the transistor Q1 during conduction is 1.5A. The forward voltage drop of the D13009K transistor as obtained from its datasheet is 1.2V (for I_c less than 15A). The duty cycle used here is 0.25 since each transistor conducts only for half of the actual duty cycle.

So the power loss during conduction in each transistor = $V_{ce} \times I_c \times D = 1.2 \times 1.5 \times 0.25$

$= 0.45W.$

The total power loss due to conduction in the primary switching circuit $P_{cond} = 0.45 \times 2$

$= 0.9W.$

B.1.4.2 Switching Losses

The datasheet for the switching transistor D13009K is not very comprehensive and does not give complete details regarding the switching characteristics of the device. The plot of switching loss for different operating voltages and currents is one such crucial information that is missing from the datasheet. The datasheet only specifies the switching times (turn on and off times) at the rated voltage and current. From the device datasheet it has been seen that for a current of 15A and rated voltage of 24V, the fall time for the current is $t_f = 0.7\mu s$. To obtain an approximate value of the switching losses it has been assumed that the turn off time doesn't vary too much with voltage and current and hence for the operating point under consideration the fall time of the current t_f is taken as 0.7μs.

Turn off losses in each of the switching transistor = $V_{ce\ (final)} \times I_{c\ (start)} \times t_f \times f_{sw}$,where $V_{ce\ (final)}$ is the final voltage that appears across the device after turn off and $I_{c\ (start)}$ is the current that was flowing through the device before the turn off started.

Turn off losses in each of the switching transistor = $154 \times 1.5 \times 0.7 \times 10^{-6} \times 7.5 \times 1000$

$= 1.2W.$

There are two switches in the primary stage and hence the total turn off losses in the switching transistors = $1.2 \times 2 = 2.4W$.

The turn-on losses were neglected because the turn-on process configures the circuit in such a way that the switches appear in series with the equivalent transformer inductance. Since this inductance opposes any sudden change in current through it, the current $I_{c\ (final)}$ which the transistor will have to switch to is almost zero and hence t_{on} loss is negligible. So the total switching loss in this stage is equal to the turn-off loss and hence the total switching loss in the input power switches is 2.4W.

B.1.5 Primary Rectifier

The primary rectifier uses a diode bridge to rectify the ac input. During 220V operation, when the voltage doubling circuit is not used, all the four diodes of the bridge are under operation whereas during the 110V mode only two of the four diodes are under active use.

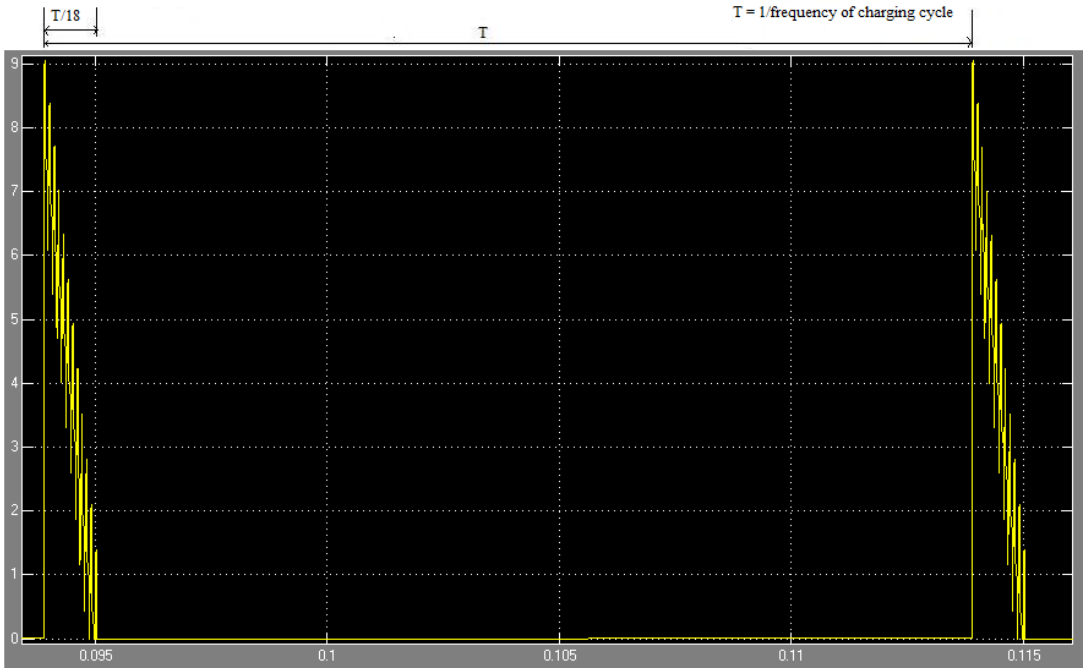


Figure 45: Current through the Diode D_x of the Primary Rectifier.

The current through one of the diodes (D_x) of the primary rectifier has been shown in Figure 45. From the above figure we can see that the diode in the primary rectifier conducts only for a small portion of the switching cycle during which the energy from the input is supplied to the dc-link capacitors. So the peak currents flowing through the primary rectifier are multiple times that flowing through the primary transistor (six here). The conduction loss in the diodes is calculated as $V_f \times I_d$ where V_f is the forward voltage drop across the diode and I_d is the current through the diode. The primary

rectifier used in this circuit is GBU-8006. The forward voltage drop of the diodes used in this rectifier as obtained from its datasheet is 1V. The average current flowing through the diode D_x during one charging cycle is $I_{d\,(avg)} = 0.5 \times 9 \times 1/18 = 0.25$ A.

So the power loss during conduction in each diode = $V_f \times I_{d\,(avg)} = 1 \times 0.25 = 0.25$W.

The switching loss in the primary rectifier diodes has been neglected as it can be seen from Figure 45 that the switching frequency of these diodes is almost an order of magnitude lower than that of the actual system switching frequency. The total power loss due to conduction in the primary rectifier in 110V mode of operation can then be computed as $P_{total} = P_{cond} = 0.25 \times 2 = 0.5$W.

B.2 Summary

The step by step computations of the loss in the various components of the Antec-350W power supply has been shown here. The loss computations are performed for the case when the power supply is supplying a PC that is operating in its idle mode (mode-1). Similarly the losses are computed for the cases where the power supply is supplying a PC operating under medium (mode-2) as well as full load (mode-3) and have been shown in Table 20 below.

Table 20: Losses in Various Elements of the Power Supply under three Modes of Operation

S. No	Lossy elements	Mode of Operation - 1	Mode of Operation - 2	Mode of Operation - 3
1	**Input Diode Bridge**	0.5W	0.86W	1.16W
2	**Input Power Switches (Conduction)**	0.9W	1.56W	2.1W
3	**Input Power Switches (Switching)**	2.4W	4.2W	5.66W
4	**Output diode Rectifiers**	8.79W	13.29W	15.86W
5	**Resistances**	4.2W	4.2W	4.2W
6	**Cooling Fan**	2W	2W	2W
	Total Estimated Loss	18.8W	26.1W	31W
	Actual Loss	20.1W	27W	33W

REFERENCES

[1] IEEE 1515-2000, "IEEE Recommended Practice for Electronic Power Subsystems: Parameter Definitions, Test Conditions, and Test Methods."

[2] IEC 62301, Ed. 1.0, "Household Electric Appliances-Measurement of Standby Power."

[3] A. Mansoor, B. Fortenbery, B. Vairomohan, T. Geist, P.M. Ostendorp, C. Calwell, R. Rasmussen, D. McIlvoy, "Generalized test protocol for calculating the energy efficiency of internal ac-dc and dc-dc power supplies," www.efficientpowersupplies.epri.com (Accessed March 12,2011).

[4] "Power semiconductor applications" Power semiconductor applications laboratory of Philips semiconductor, Hazel Grove, http://www.nxp.com/documents/application_note/APPCHP2.pdf (Accessed January 20, 2011).

[5] Mohan, Undeland, Robbins, "Power Electronic Converters, Applications and Design", 2005, Publisher: Wiley, 3rd Edition, ISBN: 978-0471226932.

[6] F.C. Schwarz, "An improved method of resonant current pulse modulation for power converters," IEEE Power Electronics Specialists Conference, pp. 194-204, 1975

[7] S.D. Johnson, "Steady-state analysis and design of the parallel resonant converter," M.S. Thesis, University of Colorado, Boulder, 1986.

[8] D. V. Jones, "Compact electrical power supply for signal processing applications," U.S. Patent 4,533,986, issued August 6, 1985

[9] Robert L.Steigerwald, "A comparison of half-bridge resonant converter topologies," IEEE Transactions on Power Electronics, vol. 3, no. 2, pp. 174-182, 1988.

[10] B. Yang, F.C. Lee, A. J. Zhang, G. Huang, "LLC resonant converter for front end dc/dc conversion," IEEE Proceedings in 17th Annual Applied Power Electronics Conference and Exposition, vol. 2, pp.1108-1112, 2002.

[11] R. Liu, I. Batarseh, C. Q. Lee, "The LLC-type and the class-E resonant converters," In Conference record of High frequency Power Conversion 1989, pp. 486-496, Naples Florida, 1989.

[12] M. Shoyama, G. Li, T. Ninomiya, "Application of common source active clamp circuit to various dc-dc converter topologies," IEEE 34th Annual Power Electronics Specialist conference, vol. 3, pp. 1321-1326, 2003

[13] F. Dong Tan, "The forward converter: from the classic to the contemporary," IEEE 7th Annual Applied Power Electronics Conference and Exposition, vol. 2, pp. 857-863, 2002.

[14] J. Zhang, X. Huang, Z. Qian, "A high efficiency fly back converter with new active clamp technique," IEEE Transactions on Power Electronics, vol. 25, no. 7, pp. 823-828, 2010

[15] U. Boeke, "High efficiency fly back converter technology," Power Conversion Conference – Nagoya, pp. 1268-1273, 2007.

[16] H. S. Choi, "Techniques to minimize the power consumption of SMPS in standby mode," IEEE 36th Annual Power Electronics Specialist conference, pp. 2817-2822, 2005

[17] J. H. Choi, D. Y. huh, "The improved burst mode in the standby operation of power supply," IEEE 19th Annual Applied Power Electronics Conference and Exposition, vol. 1, pp. 426-432, 2004.

[18] J. Lou, X. Wu, "High efficiency high integration green converter," International Symposium on Integrated circuits, pp. 53-56, 2009.

[19] A. Emadi, A. Khaligh, Z. Nie, Y. J. Lee, "Integrated Power Electronics and Digital Control," 2009, Publisher: CRC Press, ISBN: 978-1439800690.

[20] M. W. Smith, K. Owyang, "Improving the efficiency of low output voltage switch mode converters with synchronous rectification," Proceedings of POWERCON 7, p. H-4, 1980.

[21] R. S. Kagan, M. Chi, C. Hu, "Improving power supply efficiency with MOSFET synchronous rectifiers," Proceedings of POWERCON 9, p. D-4, 1982

[22] C. S. Leu, G. Hua, F. C. Lee, C. Zhou, "Analysis and design of the R-C-D clamp forward converter," Proceedings of the High Frequency Power Conversion Conference, pp. 235-246, 1992

[23] H. P. Yee, S. Meyer, K. Horiguchi, M. Wakatabe, A. Sugai, G. Dittmer, P. O. Lauritzen, "A self driven synchronous rectifier," IEEE 25th Annual Power electronics specialists conference, vol. 1, pp. 627-633, 2002.

[24] C. M. Lin, T. C. Hsu, Y. K. Chu, "Synchronous rectifier control device and a forward synchronous rectifier circuit", U.S. Patent 7,952,894, issued May 2011

[25] "Highly integrated synchronous rectification combination controller for quasi-resonant PWM controller", Datasheet Fairchild Semiconductor Corporation, http://www.fairchildsemi.com/an/AN/AN-6920MR.pdf (Accessed March 2, 2011).

[26] "Green rectifier controller device", Datasheet Texas Instruments, http://focus.ti.com/lit/ds/slusa87b/slusa87b.pdf (Accessed March 14, 2011).

[27] H. Pan, Y. C. Liang, R. Orunganti, "Design of smart power synchronous rectifier," IEEE Transactions on Power electronics, vol. 14, No. 2, 1999.

[28] C. Y. Lim, Y. C. Liang, N. Balasubramanian, "A smart power synchronous rectifier by CMOS Process", IEEE Transactions on Power electronics, vol. 25, no. 9, 2010.

[29] "Improving efficiency of synchronous rectification by analysis of the MOSFET power loss mechanism", Application Note Infineon, www.infineon.com/dgdl (Accessed March 20, 2011).

[30] T. B. Visage, "Computer Usage in Daily Life", Proceedings of Chi-2009, pp. 575-874, 2009.

[31] N. Horowitz, "Recommendations for tier 1 energy star computer specification", NRDC, Austin, Texas, 2005, www.energystar.gov (Accessed January 27, 2011)

[32] "Worldwide Quarterly Hardcopy Peripherals Tracker," IDC Press Release, August 2010, www.idc.com/getdoc.jsp?containerId=prUS22476810 (Accessed February 6th 2011).

[33] “Comparison of life-cycle greenhouse gas emissions”, www.wikipedia.org/wiki/Comparisons_of_life-cycle_greenhouse_gas_emissions (Accessed June 19, 2011).